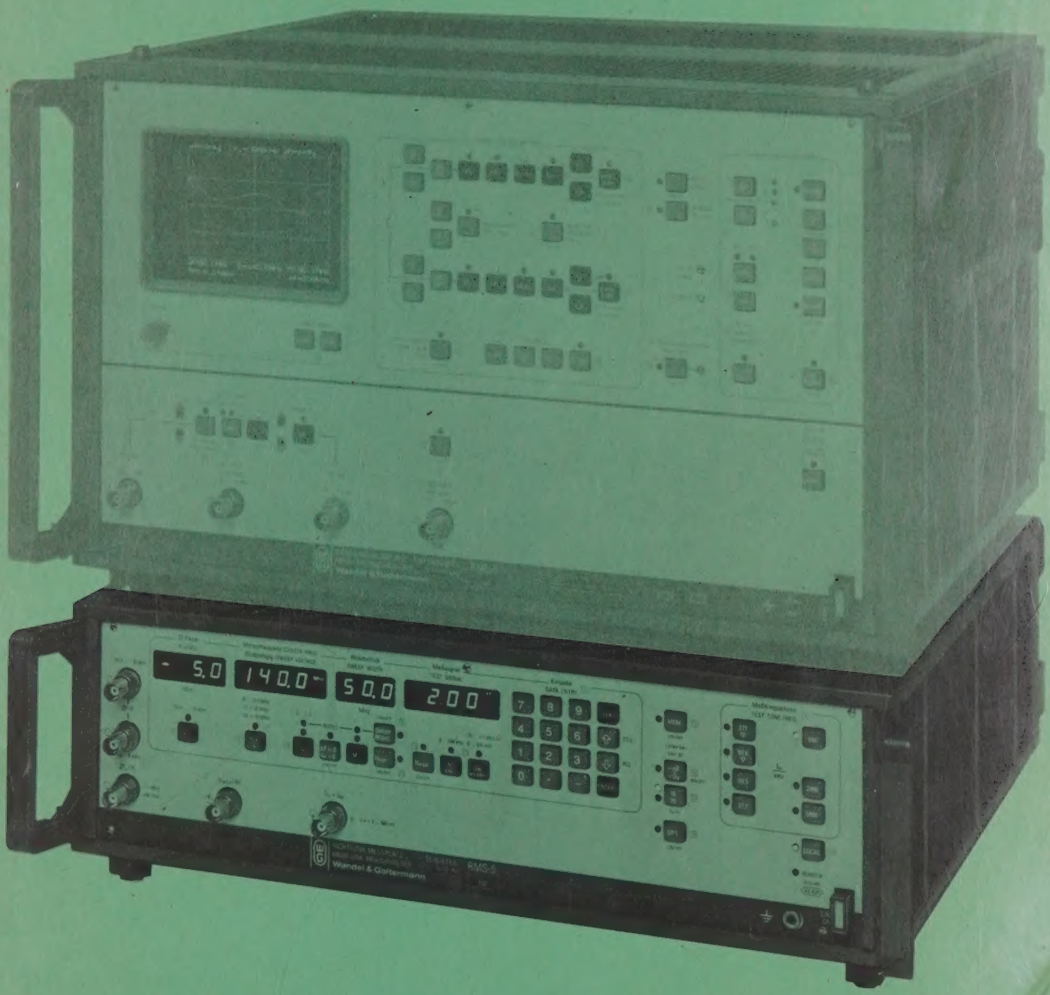
TROUBLE SHOOTING

[redacted]

Service Manual



Radio-Link Measuring Setup RM-5

Part 1 Generator Section RMS-5

BN 0916/00.83

Radio-link Measuring Setup RM-5
Part 1 Generator RMS-5

for distortion measurements on
radio-link and satellite systems

Service Manual BN 916; Series F ...

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6 PRELIMINARY REMARKS

6.1 INTRODUCTION TO SERVICING

Maintenance and repair constitute the main aspects of service work on measuring equipment. The Equipment Manual with Operating and Service Instructions and its Appendix provide all the requisite information.

The Operating Manual contains all the basic information relating to the equipment. Section 5 of the Manual describes all the non-electrical maintenance work required, such as cleaning and lubricating moving parts.

The Service Manual contains more specific information for repair work. Section 8, "Checking major technical data", contains information required for both maintenance and repair work.

The information has been compiled in such a way as to permit an experienced mechanic to carry out all the customary repair work. Work generally required only during manufacture of the equipment has been disregarded.

The Appendix contains all the general diagrams, circuit diagrams, electrical parts lists and component lists for the circuit boards. It also contains all the information required for understanding the circuit diagrams and ordering spare parts. Finally, it contains a list of the main terms used in the Appendix in German, English and French.

6.2 MEASURING AIDS

The instruments required for the tests and listed here are merely recommendations. Equivalent instruments from other manufacturers may also be used.

Instrument	Requirements	Rec. type	Manufacturer	Use, cf. Section
DC power unit	0 to 20 V	TOE 7730	Toellner	7.5.3
Digital voltmeter	3 1/2 digits	8050 A	Fluke	7.5.1, 7.5.3, 7.7.2, 7.7.4.3, 8.6
Frequency counter	up to 250 MHz	1912 A	Fluke	7.5.2, 7.5.3, 7.7.3.1, 8.2
Oscilloscope 10 : 1 Probe	bandwidth > 10 MHz	PM 3240 PM 9350	Philips	7.5.2, 7.5.3 7.7.3.1
Millivoltmeter VHF probe		411 A 11023 A	hp	7.5.3, 8.4 8.5
Milliwatt power meter Test Probe	18 Hz to 200 MHz	EPM-1 TK-10	W&G BN 564/0	7.7.3.2 7.7.5.1, 8.3, 8.7
Selective level meter	10 kHz to 100 MHz	SPM-16	W&G BN 874/xx	8.3, 8.6
Level generator	10 kHz to 100 MHz	PSS-16	W&G BN 873/xx	8.6

Table 6-1 Test equipment

Instrument	Requirements	Rec. type	Manufacturer	Use, cf. Section
Selective level meter	15 Hz to 200 kHz Bandwidth: 8 Hz	SPM-11	W&G BN 604/xx	8.5
Spectrum analyzer with probe	100 kHz - 600 kHz	8558 B 182 T	hp	7.5.3, 8.4 8.5
Signature analyzer		5006 B	hp	7.4.2, 7.4.3, 7.4.5
Receive section for RM-5	IF and f_m as unit under test	RME-5	W&G BN 917	7.7.3.3, 7.7.4.2, 7.7.5.2, 7.7.6, 8.4, 8.6, 8.7
Send section for RM-5	IF and f_m as unit under test	RMS-5	W&G BN 916	8.6
Calibrated attenuator	Z = 75 ohm 0 to 200 MHz a $\geq$ 76 dB Graduation 0.1 dB	D-2053	Siemens	8.3, 8.7
Attenuator pad	Z = 75 ohm a = 3 dB Frequency response error 0 to 200 MHz: $\leq \pm$ 0.03 dB	DG-1403	W&G BN 921/10	8.3
Attenuator pad	Z = 75 ohm a = 20 dB Frequency response error 0 to 200 MHz: $\leq \pm$ 0.03 dB	DG-1420	W&G BN 920/20	7.7.3.3
Return loss measuring attachment	Z = 75 ohm 25 kHz to 10 MHz	RFZ-5	W&G BN 394	8.6
Return loss coefficient measurement bridge	Z = 75 ohm 10 MHz to 200 MHz	RFZ-4	W&G BN 697/00.04	8.6
Matching pad	75 ohm to 50 ohm 100 kHz to 600 MHz	ZA 5075	W&G BN 925/03	8.4, 8.5

Table 6-1 Test equipment (cont.)

Designation	Type	Manufacturer	Use, cf. Section
Standard adapter board	AK-3 NF	W&G BN 901/00.13	7.4, 7.5
Special adapter board	[916-CB]	W&G 916-7076.017	7.4, 7.5

Table 6-2 Other aids and special equipment

7 TROUBLESHOOTING AND REPAIRS

7.1 SAFETY MEASURES

7.1.1 ELECTRICAL SAFETY

Protection class

This equipment is classified in protection class I to VDE 0411 and IEC Publication 348. The power cable supplied with the unit contains a non-fused earthed conductor. The mains plug may only be plugged into earthed sockets, except in specially approved rooms. The non-fused earthed conductor must not be interrupted inside or outside the equipment.

Opening the unit

Live parts may be exposed when covers are opened or parts removed with the aid of a tool. Connecting points may also be live.

The unit must be disconnected from all power sources before being opened.

If it is essential to perform calibration, maintenance or repair work on the unit when it is both open and connected to the power source, such work must only be carried out by a specially trained technician who is aware of the potential danger.

Capacitors inside the unit may still be charged even if the unit itself has been disconnected from all power sources; the circuit diagrams must be consulted.

Fuses

Only the specified fuses may be used.

Repairs, replacing parts

Repairs must be performed correctly. Particular care must be taken to ensure that the design features of the unit are not altered in a manner reducing its safety. On no account must the creepage and air paths or the insulation distances be reduced.

Only use original parts as replacements. Other replacement parts may only be used if they do not impair the safety characteristics of the unit.

Testing after repair and maintenance work

Testing the non-fused earthed conductor

Visually check for correct connection and good condition of the conductor and measure the resistance between the plug connection of the non-fused earthed conductor and the housing. The resistance should be less than 0.5 ohm. Move the connecting lead during this measurement. Fluctuations in the resistance are indicative of damage to the conductor.

Testing the insulation resistance

Measure the insulation resistance between the mains connections and the non-fused earthed conductor connection with an applied voltage of 500 V DC. Set the mains switch of the unit to "ON". The insulation resistance should be greater than 2 Mohm.

7.1.2 CIRCUIT PROTECTION

Care must be taken when handling MOS components!

MOS (metal-oxide semiconductor) components are used in this unit. They can easily be damaged or destroyed by static charges, ripple voltages from unearthed devices or other interference voltages. Damage to the gate insulation does not always result in immediate failure of a component; in many cases, this occurs only after a further period of operation. Damage by static charges can be avoided by observing the following rules:

- Wherever possible, MOS components should remain in the supplier's wrapping until used. All connections must be conductively linked until used (black, electrically conductive foam).
- The electrically conductive part of the packaging must make contact with a reference potential in the form of a conductive worktop or the frame of the unit to be repaired before unpacking the MOS components or circuit boards fitted with such components.
- Before touching MOS components, touch the conductor acting as reference potential with one hand.
- All tools and instruments, the unit to be repaired and the user should have the same potential as the conductor acting as reference potential (e.g. a conductive worktop or alternatively the earth of the unit to be repaired). For this reason, first make contact between the reference potential and the tools for handling MOS components. The handles of these tools must not be insulated.
- If work is being carried out on a circuit board or part of a unit separate from the rest of the unit and not lying on a conductive worktop, connect the earth of the circuit board, etc. to the reference potential.

Damage caused by ripple voltages during soldering work can be avoided by establishing a permanent connection between the soldering iron and the earth of the unit being repaired.

MOS components include the letters MOS, CMOS or MOSFET in the component designations of the electrical parts list.

7.1.3 SOLDERING INSTRUCTIONS

It is recommendable to use thin solder with little flux. Note the following points:

- Soldering time for all components: max. 5 seconds
- Soldering temperatures: max. 260 °C
- Avoid flux splashes on switch contacts
- Ensure that flux is not spilled onto contact-making surfaces when soldering switch contacts or other electromechanical components.

Desoldering components with numerous connections:

The best method by far is to remove the solder of each individual connecting wire by suction using special-purpose desoldering equipment. Move the wire back and forth gently while desoldering to check that each individual connection is free. Do not use force!

Throughplatings are sensitive to tensile stresses during soldering!

7.1.4 DEVICE MARKINGS

The following instrument data are required for all enquiries, when ordering spare parts or for checking whether these Service Instructions apply for the unit to be repaired:

Type designation, designation of the specific model,
options installed, serial index and instrument number.

The locations of the individual markings are illustrated in Fig. 7-1.

7.1.4.1 Identification of Software Packages

Software packages are identified via the signature list (BV).

- Instruments with drawer for abridged operating instructions: the signature list with designation number is accommodated in the drawer.
- Instruments without drawer: the signature list is located inside the device. Section 7.3.1.1 describes how to find the list. The signature list is marked by a label on the rear cover panel.
- Options: a signature list generally cannot be included due to lack of space. In such cases, it is included with the list of the basic unit. The list number, however, is marked on the option itself.

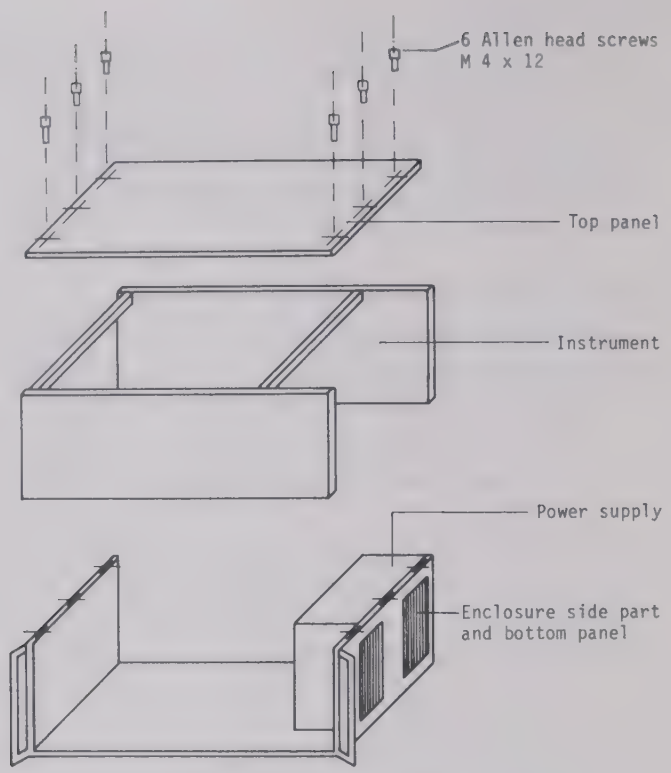
The signature list must be updated or replaced if options or new software are retrofitted.

7.1.5 DISMANTLING THE DEVICE

Disassembly of the device is illustrated in Fig. 7-1.
The screening boxes and frames are illustrated in Fig. 7-2.

After removal of the 6 upper Allen head screws, the instrument is lifted upwards and out from the enclosure. The power supply remains in the enclosure. It is, however, connected to the instrument by a wiring harness.

Tool:
Allen wrench, Sw = 3
(see back panel)



Front view of instrument

Back view of instrument

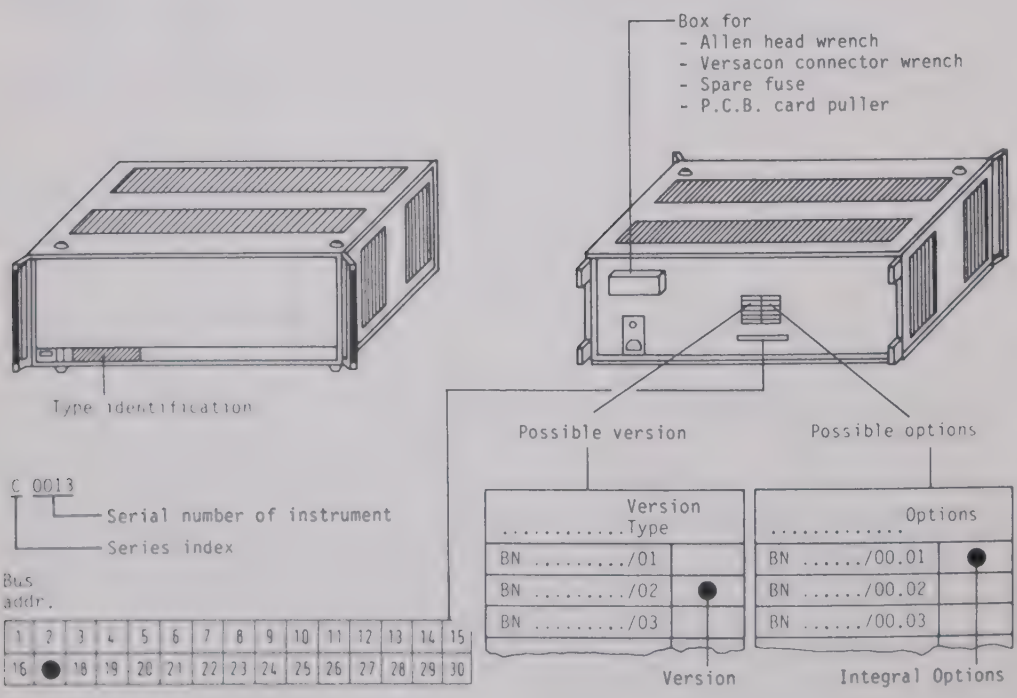
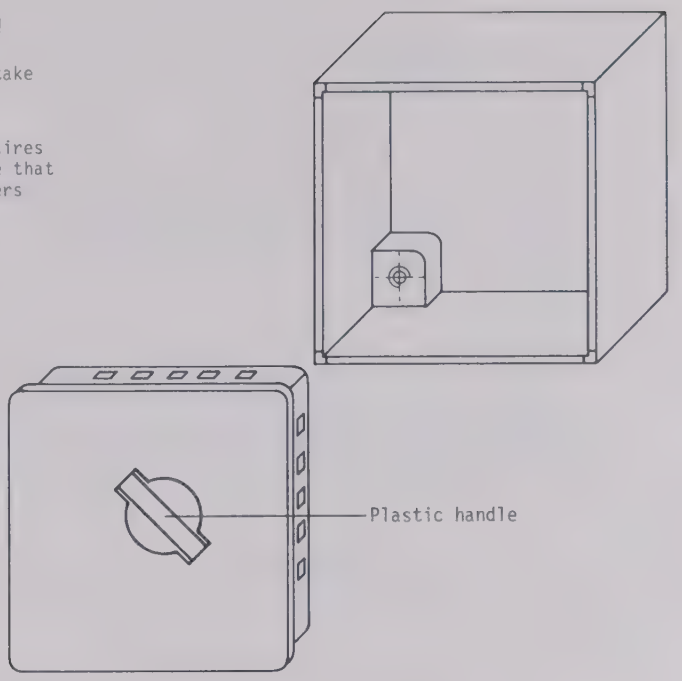


Fig. 7-1 Dismantling the device and device markings

Removal of cover from screening boxes and frames

The plastic handle is used to take the covers off from the frames and boxes.

Caution: replacing a cover requires attention to make sure that the thin contact fingers are not damaged.



Disassembly of circuits from screening boxes and frames

The stand-off screws or spacers to which the printed circuit board is attached, and all chassis-ground screws should be removed. Then the printed circuit board is removed by the card puller.When replacing the circuit the contact pins must be protected by assuring the p.c.b. is exactly parallel to all pins before the p.c.b. is pressed home.

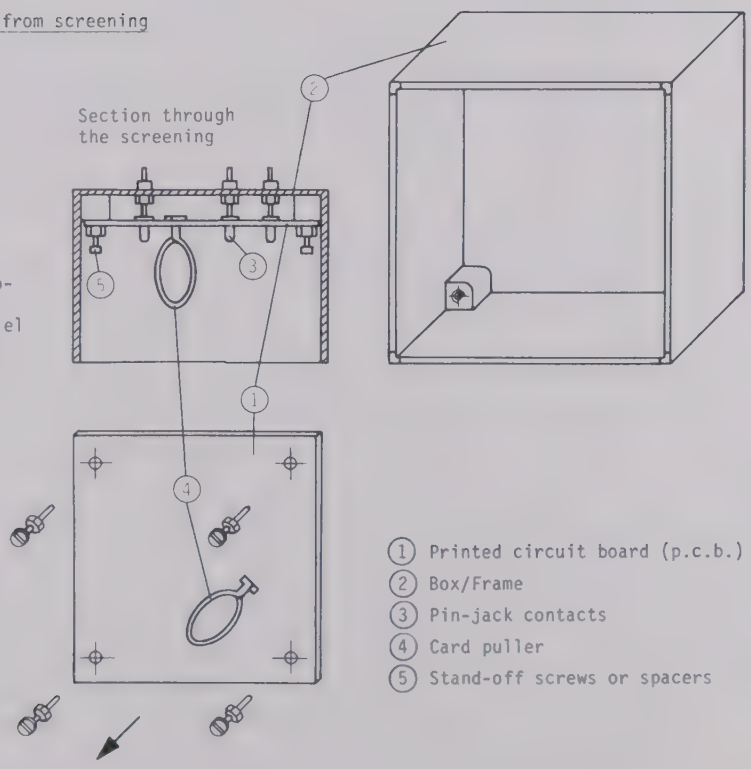


Fig. 7-2 Screening boxes and frames

7.1.5.1 Removing the device from the enclosure

The device is removed from the complete unit as follows:

- Place the unit in operating position.
- Remove the cover after unscrewing the six Allen head screws using the key supplied.
- Break the cable connections between the device and the power supply unit.
- Carefully lift the device up and out of the enclosure.

Note: Remove the spare fuses from the recess on the rear of the enclosure before lifting out the device.

If troubleshooting was performed immediately before repairing the instrument, it may be assumed that the instrument is dismantled and positioned as described in Section 7.1.5., i.e. the device is virtually exposed. Only the cable connections between the device and the power supply unit need be broken before the device is disconnected from the right-hand side panel by sliding it to the side in the guide grooves. Remember to remove the spare fuses as noted above.

7.1.5.2 Removing the power supply unit

The power supply unit and right-hand side panel form a single unit. They are removed as follows:

- Place the instrument on its left-hand side.
- Unscrew the screws connecting the right-hand panel with the upper and lower covers.
- Place the instrument in operating position and remove the upper cover completely.
- Break the cable connections between the power supply unit and the device.
- Lift the device out of the enclosure until the right-hand panel and the power supply unit can be removed. Remember to remove the spare fuses as noted in Section 7.1.5.1!

7.1.5.3 Removing printed circuit boards

The printed circuit boards are housed in enclosed, metallized plastic screening cans. The cover of the box must be removed using the plastic tabs provided before the circuit boards can be removed.

Desolder the connecting wires and unplug all connections on the circuit board; then remove all the cross-head screws securing the circuit board. Finally, lift the circuit board out of the box: most of the boards are fitted with a special board extractor.

7.1.5.4 Removing plug-in boards

Control board (9) [916-BP] and CPU board (90) [965-A]

- Release the split rear panel.
- Remove the plug-in boards.

IEC-625 interface (91) [958-D]

- Undo all screws.
- Remove the interface board together with the cover panel.

7.1.5.5 Removing the front panel

The front panel must be removed in order to remove the card rack [916-BQ].

- Remove the device.
- Remove the printed cover panel (five fillister head screws).
- Break the RF connections between the calibrated attenuator and the front panel as well as RF connections 8 ST 1, 16 ST 1, 16 ST 9 and 18 ST 3.
- Disconnect the front panel from the device (four countersunk screws).
- Disconnect the ribbon cable ST 10 from the card rack.

7.1.5.6 Removing the card rack [916-BQ]

The front panel must be removed before removing the card rack (cf. Section 7.1.5.5).

- Draw the plug-in boards (control board [916-BP], CPU board [965-A] and IEC-625 interface board [958-A] out from the rear of the instrument.
- Disconnect the card rack from the device (six cross-head screws).
- Disconnect the remaining plug connections.

7.1.5.7 Removing the upper mother board [916-BV]

The cover must be removed from the instrument before the upper mother board can be removed.

- Remove the rear cover panel (five fillister head screws).
- Unscrew the rear fastening screws for the upper mother board (two countersunk screws).
- Break RF connections 6 ST 1 and 8 ST 3 as well as the connection to the card rack (ST 13).
- Unscrew the fastening screws at the side (six cross-head screws).
- Unscrew the front fastening screws for the upper mother board (two cross-head screws).
- Raise the rear of the assembly; hold it at an angle and draw it back a short distance out of the device.
- Disconnect the remaining connections to the upper mother board.
- Remove the board completely.

7.1.5.8 Removing the lower mother board [916-BU]

The bottom panel of the instrument must be removed before removing the lower mother board.

- Remove the rear cover panel (five fillister head screws).
- Remove jack [35] $\hat{U}_{AEXT}$ (two countersunk screws).
- Unscrew the rear fastening screws for the lower mother board (two countersunk screws).
- Break RF connections 16 ST 1, 16 ST 9 and 18 ST 3.
- Unscrew the fastening screws at the side (six cross-head screws).
- Unscrew the front fastening screws for the lower carrier board (two cross-head screws).

- Raise the rear of the assembly; hold it at an angle and draw it back a short distance out of the device.
- Undo remaining connections to mother board.
- Remove the board completely.

7.1.5.9 Removing the attenuator set FED-2

- Remove the front panel as described in Section 7.1.5.5.
- Break the RF connection to the calibrated attenuator.
- Disconnect the control lead (ribbon cable) from the attenuator set board.
- Unscrew the attenuator set from its mounting plate (three cross-head screws).
- Remove the attenuator set from the device.

7.1.5.10 Soldering and desoldering chip components

Tools required:

Thermostat-controlled soldering iron with forked bit, e.g. Weller-Magnastat (50 to 80 W) with Group 5 (up to 260 °C) or Group 6 (up to 310 °C) bit, or an adjustable soldering iron, Type Zeva G 5 T (65 W) set to 280 °C.

Type C 3 solder (dia. 1 mm) with 1.5% colophony must be used.

The maximum permissible temperature for soldering and desoldering is 240 °C at the soldering joint. This temperature is not exceeded if the soldering time is kept as short as possible (max. 3 s).

For soldering work, the soldering joint on the component side of the board must be presoldered. Then position the contact surfaces of the component on the soldering joint. The two soldering joints on the conductor path are heated simultaneously using the forked bit; the bit must not touch the component. If necessary, the component can be held in position during soldering with the aid of a wooden pin. If two chips are to be soldered close together, always allow the first solder to cool before soldering the second chip. Chip capacitors may only be picked up on the contact surfaces with metal pincettes.

7.2 ASSEMBLY LAYOUT AND LEVEL MEASURING POINTS

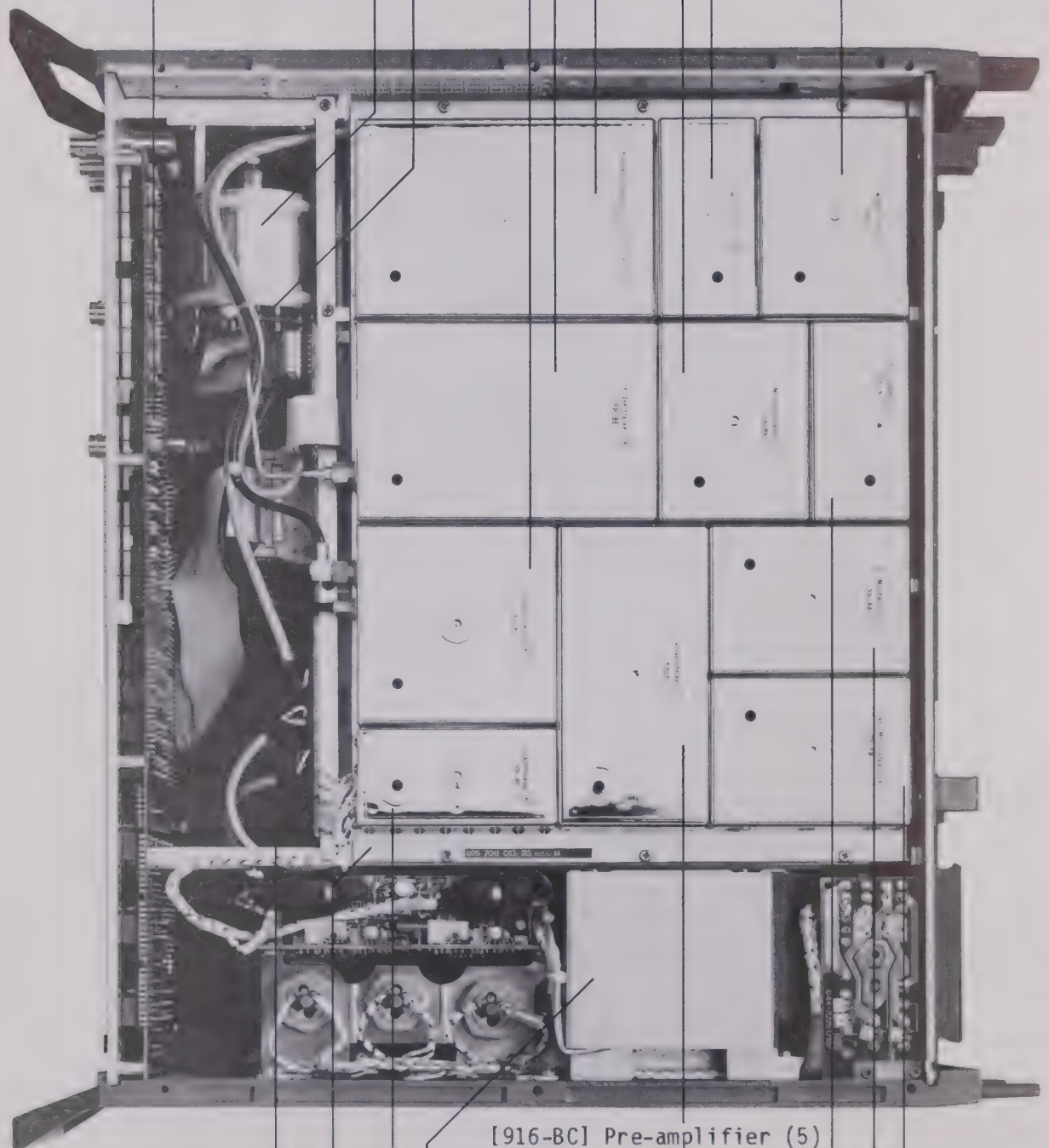

[916-BB] Output amplifier (6)
[916-BD] Frequency divider (8)
[916-BJ] Detector (12)
[809-D] calibrated attenuator (control board)
[916-BN] Modulation oscillator (2)
809/03 calibrated attenuator (FED-2)
[916-BL] U_M changeover unit (16)
[916-BM] Front panel board (7)
[916-R] Sweep oscillator (10)
[916-BC] Pre-amplifier (5)
[916-BQ] Board rack (17)
[696-N] 1 GHz low-pass filter (11)
[916-BV] Upper mother board
[916-BA] Mixer (3)
[916-BE] Discriminator (8)
[916-BW] 460 MHz low-pass filter (4)
844/3 Standard power supply 3 (line filter, transformer unit, 5 V/± 12 V control and data recovery) (1)

Fig. 7-3a RMS-5 generator; assembly layout, top view

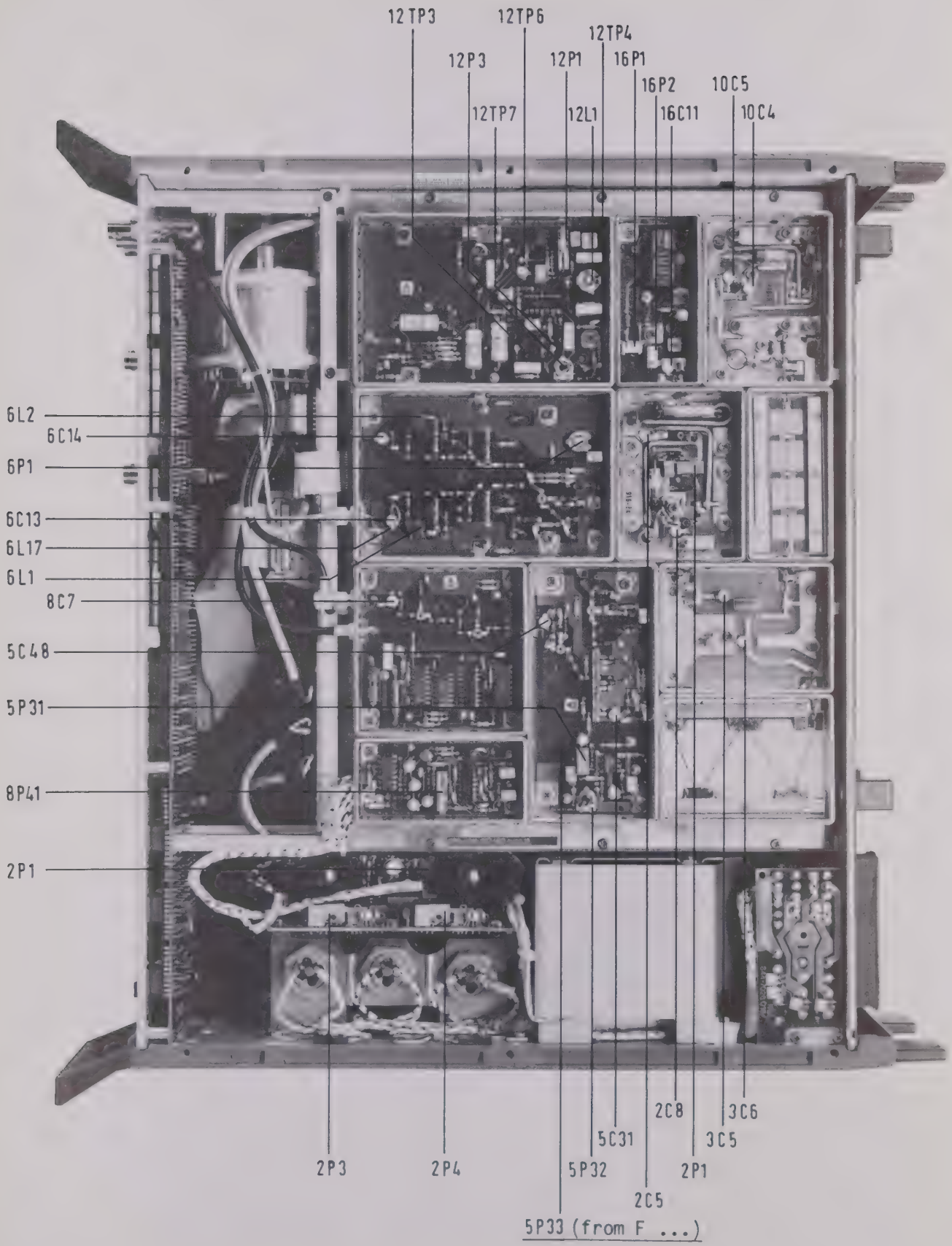


Fig. 7-3b Layout of the alignment controls and test points, top view

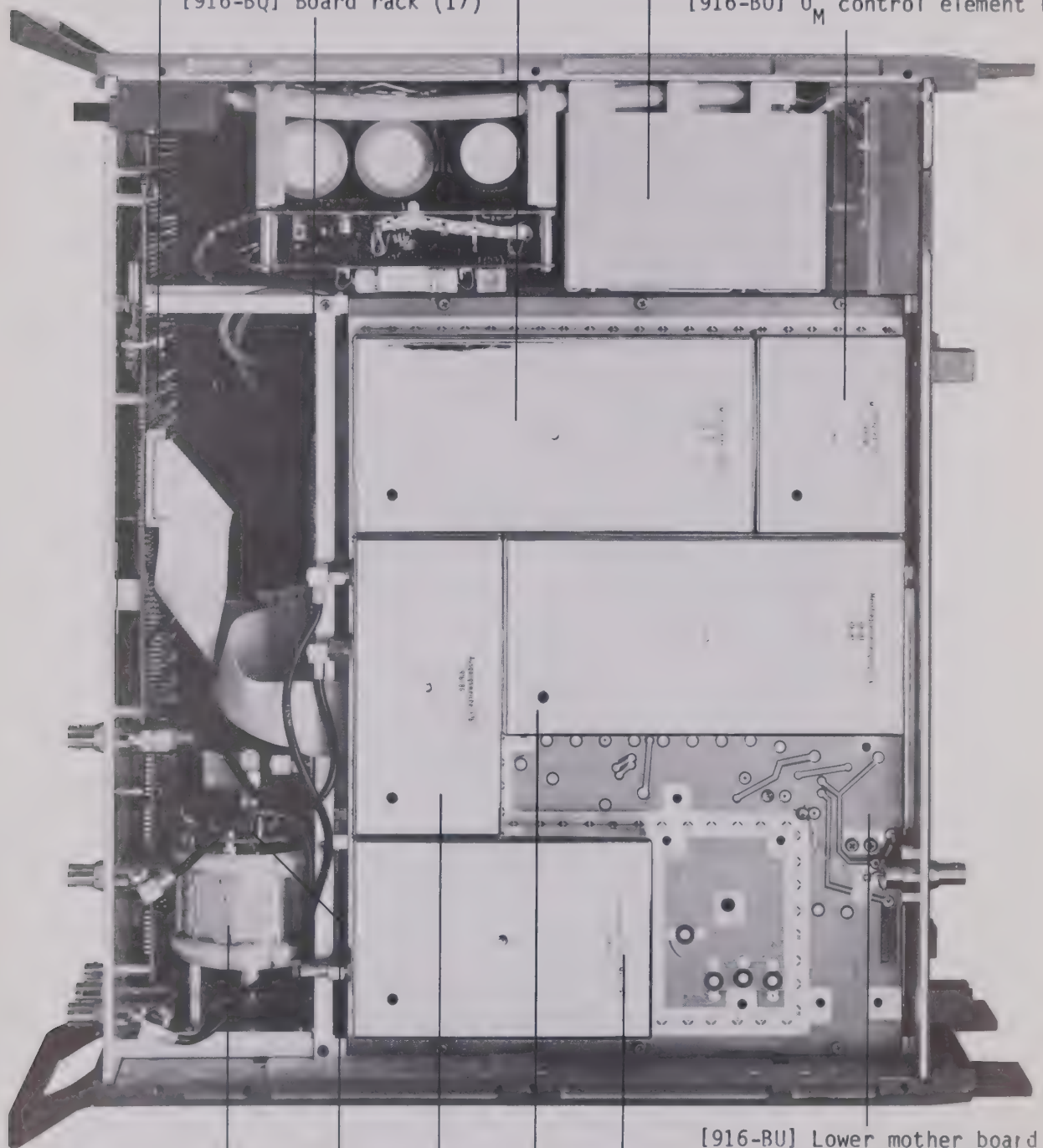

[916-BZ/CA] U_M amplifier (15)
844/3 Standard power supply 3 (line filter, transformer, 5 V/± 12 V control and data recovery) (1)
[916-BM] Front panel board (7)
[916-BQ] Board rack (17)
[916-BO] U_M control element (15)
[916-BU] Lower mother board
809/3 Attenuator set (FED-2)
[809-D] Calibrated attenuator (control board)
[916-BG] Output filter (16)
[916-BX/BY] Test frequency generator (14)
New [916-CC] IF calibrating generator 35/70/140 MHz (18) (optional)
Old [916-H] IF calibrating generator 35/70 MHz (18) (optional)

Fig. 7-4a RMS-5 generator; assembly layout, bottom view

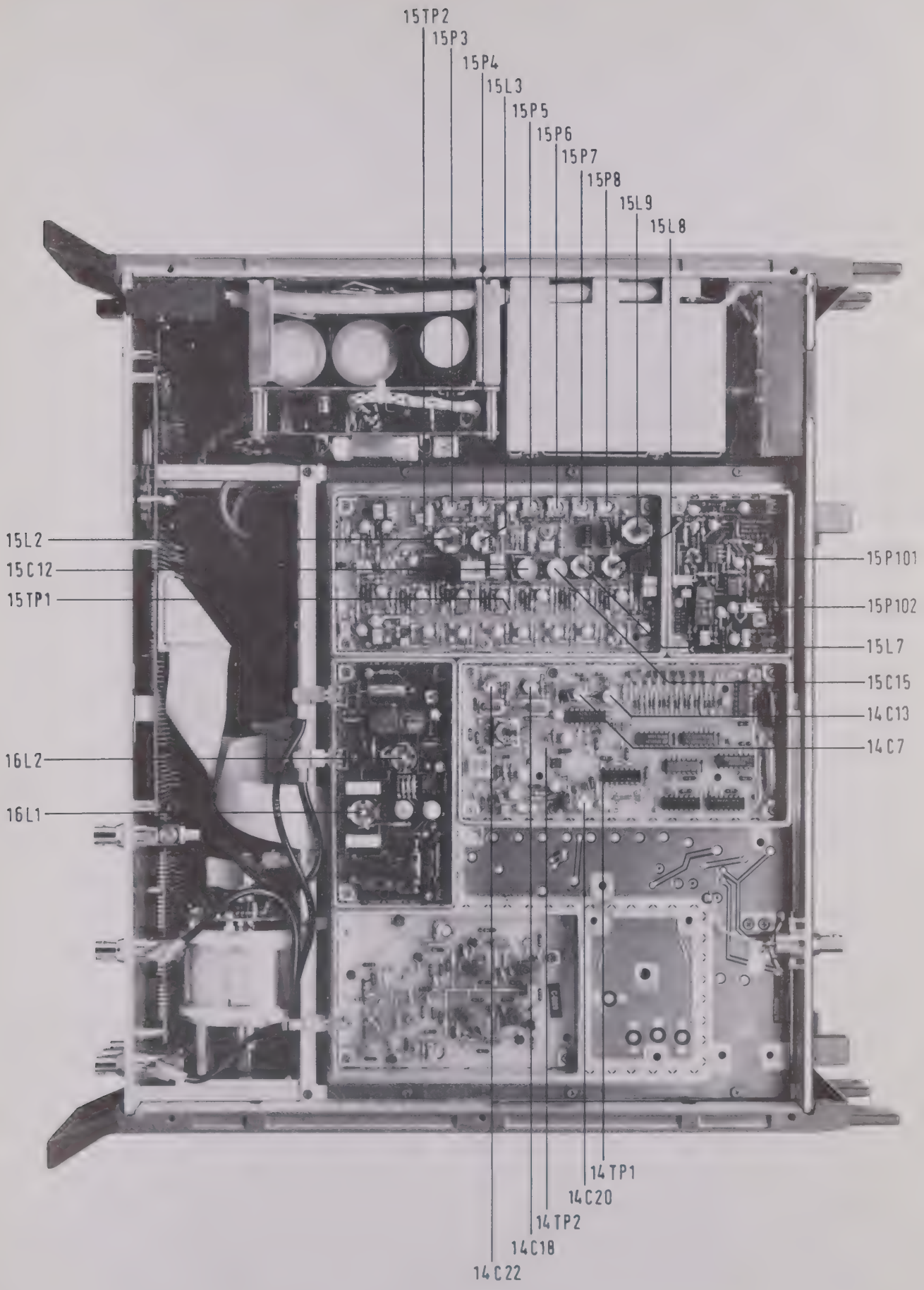


Fig. 7-4b Layout of the alignment controls and test points, bottom view

Fig. 7-5 RMS-5 generator; assembly layout, rear view

[916-BP] Control board (9)

assembly layout, rear view

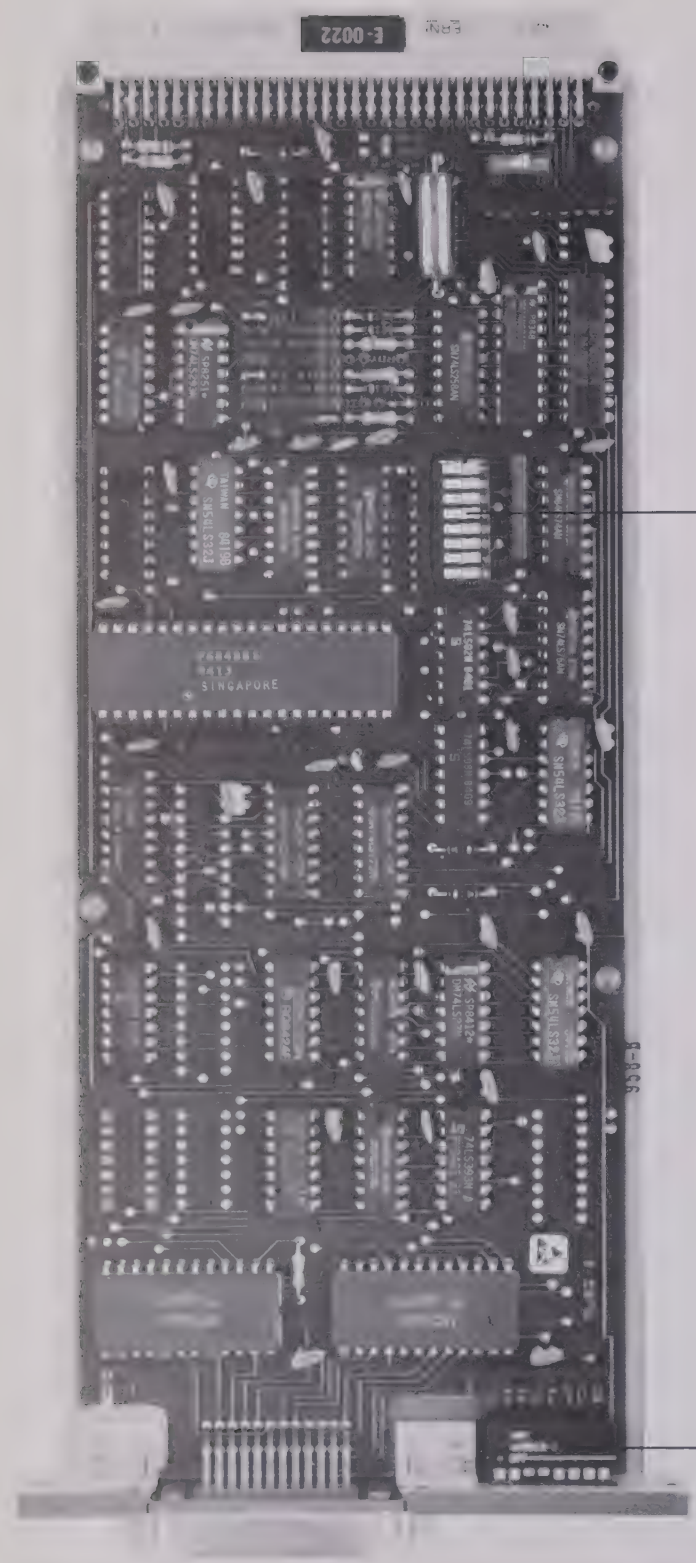


Fig. 7-6 <IEC 625> interface [958-B]; switch layout

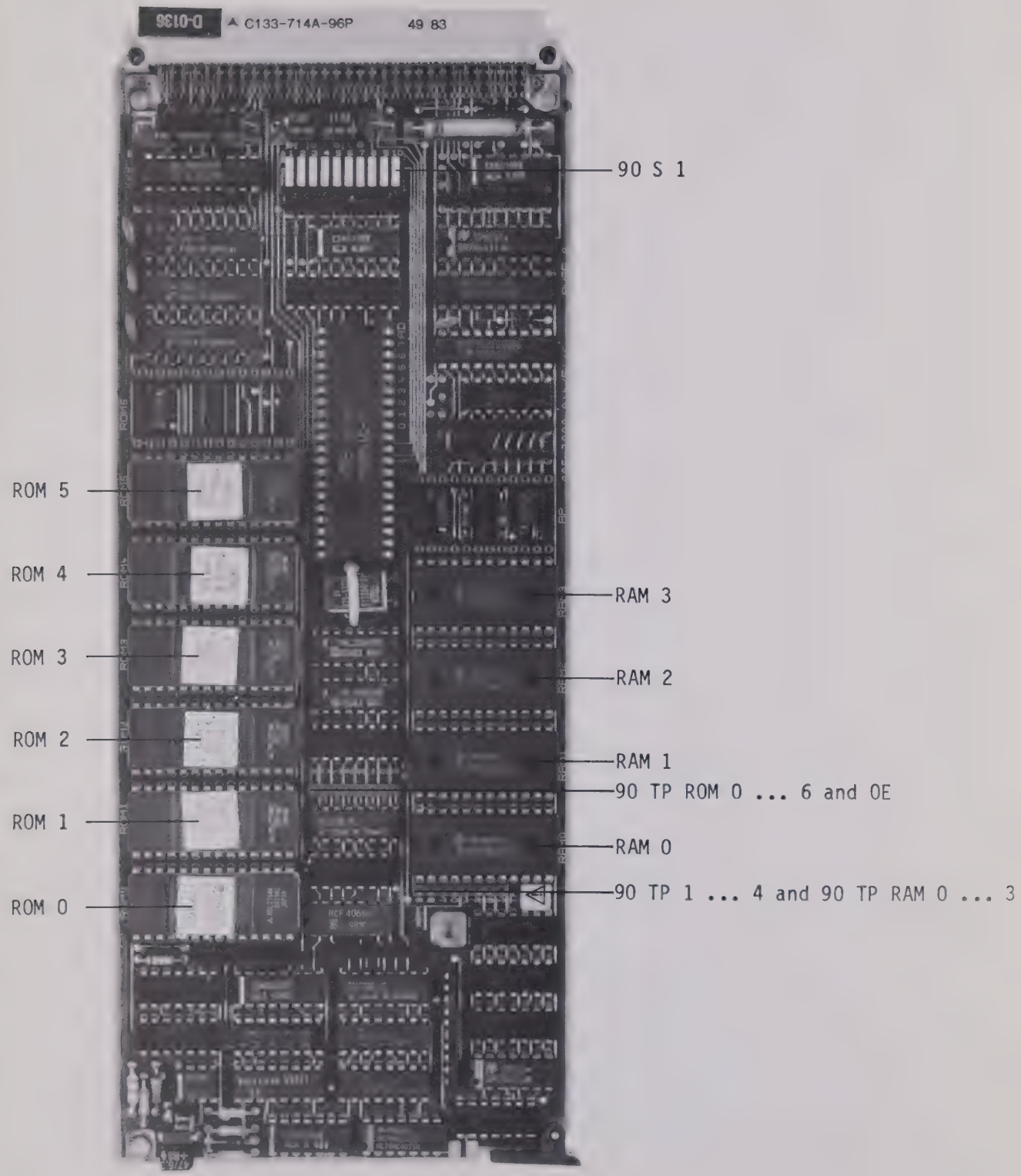


Fig. 7-7 CPU board [965-A]; layout of switches, test points, RAM and ROM modules

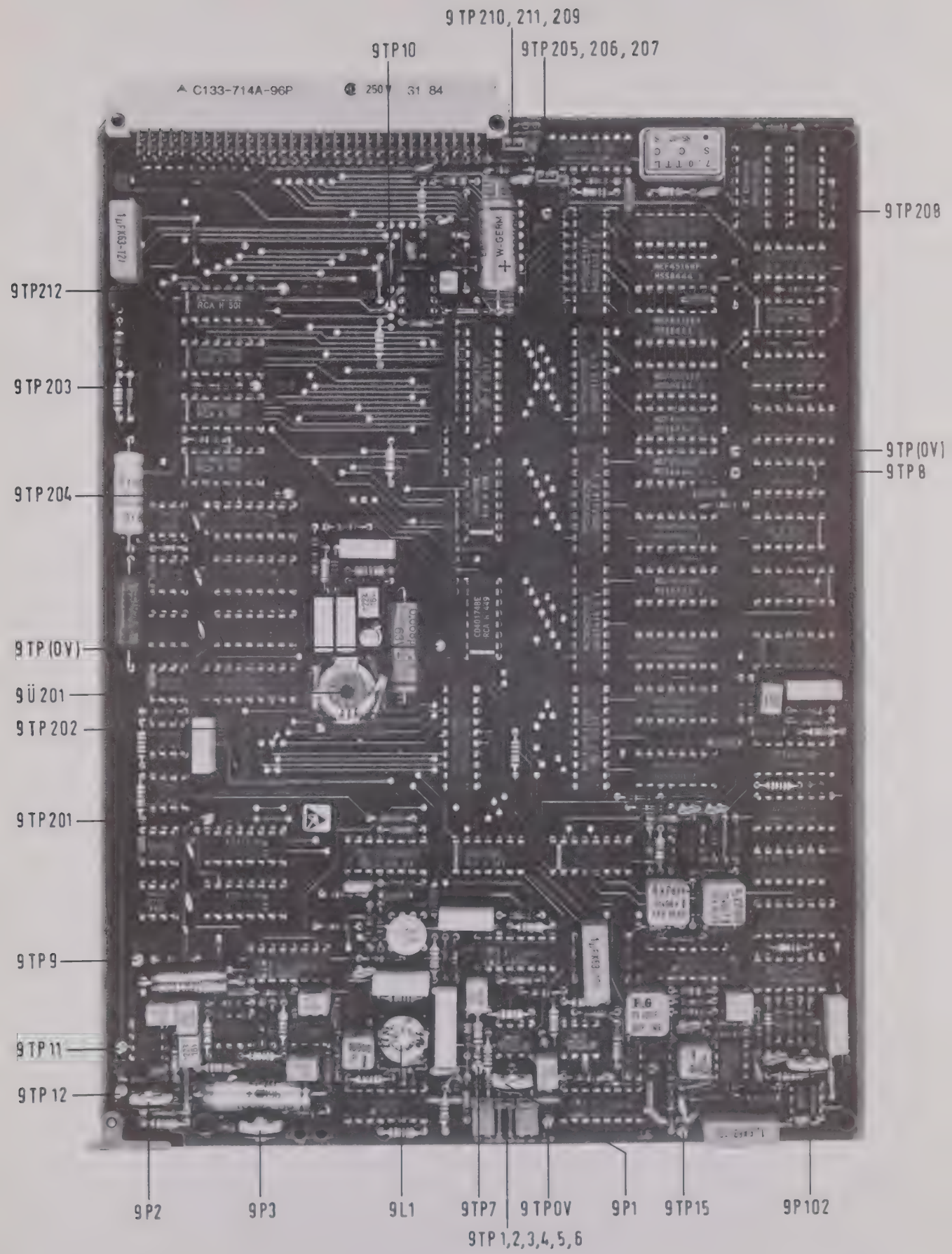


Fig. 7-8 Control board (from series F onwards), layout of alignment controls and test points.

7.3 TROUBLESHOOTING

7.3.1 INTRODUCTION TO NEW MEASUREMENT AND TEST PROCEDURES

7.3.1.1 Signature analysis

Digital signal sequences of any length can be checked easily and unambiguously using a signature analyzer (e.g. hp 5004A/5005A/5006B). Unchanging signatures (4-digit, pseudo-hexadecimal notation) are produced on the lines under test when defined and repeatable bit patterns are present in relation to a time frame (= START/STOP frame). The microprocessor is forced to generate such bit patterns by a stimulus program or external control.

Data lines AD$\emptyset$ ... AD7 are connected to +5 V via a switch on the CPU board. Line AD7 is additionally connected to signal $\overline{RD}$ via a Schottky diode, thus triggering "processor free running". Data lines AD$\emptyset$ to AD6 = HIGH and AD7 $\cong$ $\overline{RD}$ = LOW during the read operation. The free running instruction is thus 7FH $\cong$ MOV, A. If the highest-order address bit A15 is used as the time frame = START/ STOP frame, the processor increments the entire address range from $\emptyset\emptyset\emptyset\emptyset$ to FFFF. Each address line consequently generates a unique signature. A signal satisfying the time condition ($\overline{RD}$ in the case of microprocessor 8085) is used as the CLOCK signal. It is essential that the timing of the signals CLOCK, DATA, START and STOP be correct in order to prevent unstable signatures. Two frequently occurring signatures are briefly described below.

The signature of the $\emptyset$ V line is always 0000, regardless of the START/STOP frame. The signature of the +5 V line is designated the "CHARACTERISTIC SIGNATURE". The characteristic signature indicates whether the START/ STOP frame is correctly connected and whether the edges of the START/STOP frame are correct. It may also be assumed that the microprocessor is working.

If the frame signature appears on an address or data line, this indicates a short to the supply voltage; if the signature 0000 appears, a short to chassis-ground has been made. If two address or data lines have the same signature, it is highly probable that a connection has been made. If the address range is limited to the ROM addresses during free running (START/STOP frame corresponds to the appropriate chip select signal), a bit stream corresponding to the ROM content is produced on the data lines.

The list of ROM signatures is enclosed with the device; it is always in the left-hand side panel.

Unlike the ROM with unalterable data, the contents of the RAM (and of the I/O area) depend on the momentary "status" of the test device. Verifiable data must be input to the RAM area and the I/O ports addressed periodically before meaningful signatures can be obtained. Only a program, the stimulus program as it is known, is capable of this. Such programs can be called up via a switch. When the device is switched on, the microprocessor first executes the initialization routine, polling the switch position $\cong$ bit pattern to call up certain stimuli and continuing the program at the point defined in this manner.

7.3.1.2 Standard setup and integrated test software

The microprocessor system must be re-initialized after removing the power supply unit, the CPU board, disconnecting the battery, etc., since important data required for correct operation have been lost from the buffered RAM memory. The data in the RAM memory can be restored using the available initialization programs.

The control system of the RMS-5 has four initialization modes:

I When the device is switched on, the microprocessor system normally notices if the battery voltage is too low, or if RAM data have been modified as a result of this and runs an initialization routine.

II Initialization can be triggered manually by pressing the /LOCAL/ button [19] until the standard setup appears on the displays after the device is switched on.

III The two contact surfaces accessible on the CPU board after opening the rear panel can be briefly connected after switching on the device.

IV If -CLEAR- wire-link or switch is closed, initialization can be called up via the IEC bus using the "IFC" command.

The device is not initialized when setting the standard setup, an operational setting being defined instead. The standard setup can be set manually by pressing: /MEM/, /0/, /RCL/. It can be called up via the IEC bus using "INI" or "RCLØ".

The following parameters are set when initialization is performed or the standard setup is selected:

IF		: 70 MHz
Level		: 0 dBm
$\hat{U}_A$		: 1 V
Sweep width		: 0.5 MHz
Sweep reduction		: OFF
Test signal	Δf	: 100 kHz
Test signal	U_M	: 100 mV ≙ -8.7 dBm
f_A		: low sweep frequency (18 Hz)
f_m		: 500 kHz or 555 kHz
$\hat{U}_{A\ EXT}$		: OFF
$U_{M\ EXT}$		: OFF
Sweep		: ON
GAP		: OFF
Option		: OFF

Table 7-1 Standard setup

The control section is faulty if it is not possible to obtain the standard setup. Trouble-shooting is described i Section 7.4.

Some general information on the self-test capabilities of the RMS-5 is given below. Together with a minimum of signature analysis, some of these self-tests will suffice to localize a fault on one of the assemblies in the processor control system. The fault can then be eliminated by replacing the board concerned.

A number of convenient self-test programs are available for the analog section of the device. Together with the detailed instructions on troubleshooting, they allow faults to be localized in the analog assemblies and on the control board. Signature analysis is required to eliminate faults on the control board.

Extreme care must be taken when repairing faults on the two RF oscillators (sweep oscillator and modulation oscillator). All major faults must be repaired by the manufacturer. Re-alignment is essential whenever components are replaced; this can only be performed with the requisite precision by the manufacturer. Incorrect alignment will produce errors in the results of distortion measurements and seriously impair the noise characteristics of the device.

The test routines described below are started by setting the appropriate combination on switch S1 of the CPU board when the device is switched off and then switching on the device. A test routine is started in the same manner if the appropriate combination has been set on service switch S1 and the CLEAR function triggered for the CPU board (short the contact surfaces).

In the event of a fault, the "summary self-test", which is also performed when the device is switched on, will cause an error number to appear on the display, provided that this output channel is functioning correctly.

7.3.2 INTEGRAL TEST AIDS IN THE FORM OF TEST ROUTINES

A. Tests for CPU board BN 965

	Setting on switch 90 S1 1 2 3 4 5 6 7 8 9 10	
RAM test (contents are modified)	x x x x x x x x x	ON
	x x	OFF
IEC test	x x x x x x	ON
	x x x x	OFF
I/O test	x x x x x x x x	ON
	x x	OFF
RAM test (contents not modified)	x x x x x x x	ON
	x x x	OFF
ROM test	x x x x x x x x	ON
	x x	OFF
Summary self-test (with error message via display)	x x x x x x x x	ON
	x x	OFF
Monitor program for "MONEX"	x x x x x x x x	ON
	x	OFF
Normal operation: Series I	x x x x x x x x	ON
	x x	OFF
Series II	x x x x x x x	ON
	x x x	OFF

Table 7-2 Test routine for CPU board

The CPU board tests are repeated cyclically until a fault is found; the test sequence then stops. The SOD signal of the microprocessor 90 IC 41.1 is used as indicator: if the SOD signal rests on a logic level, this means that the program has been interrupted because a fault has been detected.

The summary self-test comprises a ROM test, an I/O test and RAM test which does not alter the contents of the RAM. The first fault found in a summary self-test is displayed on the centre frequency display. The test routines generate the following error codes:

No error:	No display	
ROM error:	Ø1.Øi	; i = Ø ... 5 ≙ ROM Ø ... ROM 5
RAM error:	(test without modification of content)	
	Ø2.ji	; i = Ø ... 3 ≙ RAM Ø ... RAM 5
		j = 0 : cell error
		j = 1 : address error (AØ ... A1Ø)
		j = 2 : address error (A11, A12)
I/O error:	Ø3.ØØ	

The summary self-test as described above can also be initiated by pressing button /1/ [2] when the device is switched on.

B. Test routines for other assemblies

		Setting on switch 90 S1 1 2 3 4 5 6 7 8 9 10	
I	Frequency control linearity	x x x x x x	ON
	(self-test)	x x x x	OFF
II	Centre frequency control	x x x x x x x	ON
	(self-test + signature analysis)	x x x	OFF
III	I/O ports (signature analysis)	x x x x x x	ON
		x x x x	OFF
IV	D/A converter: $\hat{U}_A$	x x x x x x	ON
		x x x x	OFF
V	D/A converter: $\Delta\hat{F}$	x x x x x x x	ON
		x x x	OFF
VI	D/A converter: Δf, U_M	x x x x x	ON
		x x x x	OFF
VII	D/A converter: IF centre	x x x x x x	ON
		x x x	OFF
VIII	D/A converter: detector	x x x x x x	ON
	control voltage	x x x	OFF
IX	D/A converter:	x x x x x x x	ON
	control voltage, IF control	x x	OFF

Table 7-3 Test routine for device hardware

Functional description of the above test routines:

I Frequency control linearity

When 9 TP 2 - 9 TP 3 and 9 TP 5 - 9 TP 6 have been connected, two voltages are connected one after the other to the input of the frequency control circuits. The difference between the two voltages is known (approx. 1 V). The IF output frequency corresponding to the respective voltages is determined by the counters of the centre frequency control assembly.

The linearity is calculated and displayed as the quotient of the IF output frequency difference and the input voltage difference. The linearity values for the IF bands 35 MHz, 70 MHz and 140 MHz are displayed from left to right. The linearity display for 70 MHz has the highest resolution, since individual alignment is performed in this band (nominal value 12.00).

This test routine checks the entire frequency control and centre frequency control.

II Centre frequency control

The same frequency f_{REF} = 350 kHz is applied to both counter inputs after connecting 9 TP 206 - 9 TP 207. The gate time of the counter is derived from the same generator, meaning that the counter values for each measurement are defined exactly. The test routine polls both counter values, compares them with the set-point values and outputs a message on display 2. The entire assembly is also made accessible for signature analysis (stimulus MFR, MFR-1) by the cyclic sequence.

Error messages: No error detected: 10.00
Error detected: 10.01

III I/O ports

This test routine is a stimulus program for testing via signature analysis and comprises two areas:

Stimulus PORT 1: Addresses of all output gates (WR gates) and writes test patterns to the output gates.

Stimulus PORT 2: Addresses of all input gates (RD gates).

IV D/A converter

The respective D/A converter is incremented and set so that a sawtooth or sinusoidal signal with sawtooth envelope is obtained at the output.

7.3.3 FAULT LOCALISATION

I CPU board test

II Front panel test by checking the response to keyboard inputs

III Function check of the BB parameters
Sweep voltage, sweep frequency
Test voltage, test frequency

IV Function check of the IF parameters
IF level
Centre frequency
Sweep width
Test width

V Function checks of the EXT functions.
$\hat{U}_{A\ EXT}$, $U_{M\ EXT}$

I If it is suspected that there is fault on the CPU board, the summary self-test can be run by pressing button 1 on the input panel [2] until the displays are cleared when the device is switched on. This summary self-test is repeated cyclically until a fault is detected. The fault is then indicated in coded form on the centre frequency display. The test routine is interrupted, since any further faults cannot be detected.

II When the device is switched on, the LEDs, digital displays and unit LEDs light up for approx. 3 s. Some LEDs which are only activated alternatively in normal operation do not light up with full brightness.

III The function check of the BB parameters $\hat{U}_A$ and U_m may be performed using an RME-5, or an oscilloscope and frequency counter.

IV The function check of the IF parameters can be performed very simply using only the RME-5. The IF level can be checked using an RF level meter, the centre frequency without sweep width using a suitable frequency counter.

V The function check of the EXT functions may be performed using the internal BB signal and the RME-5.

7.4 TROUBLESHOOTING THE CONTROL SYSTEM

Settings of switch 90 S 1 for normal operation:

	1	2	3	4	5	6	7	8	9	10	
f_M series I	x	x	x	x		x	x	x		x	ON
					x				x		OFF
f_M series II		x	x	x		x	x	x		x	ON
	x				x				x		OFF

7.4.1 PROCEDURE

- Troubleshooting the ROM area using test routine and/or signature analysis.
- Troubleshooting the RAM area using test routine.
- Troubleshooting the I/O area of the CPU board using test routine.
- Troubleshooting the I/O area of the control board using signature analysis.
- Troubleshooting the IEC bus interface.

7.4.2 ROM TEST

Switch 90 S 1

1	2	3	4	5	6	7	8	9	10	
x		x	x	x	x	x	x		x	ON
	x							x		OFF

The test routine calculates the checksums for the individual EPROMs and compares these values with those stored in EPROM Ø. Any discrepancy is identified as an error and the routine interrupted with HALT status. The SOD signal 90 IC 41.4 remains at one logic level.

Special feature: ROM 5 contains only device-specific data which vary according to type and option. ROM 5 is therefore not included in the ROM test. Where appropriate, the data may be checked via signature analysis.

In the event of an error, check the following:

- $\overline{\text{RESET IN}}$ = LOW
- TRAP, HOLD = LOW
- READY = HIGH
- Clock = 4 MHz

Signatures for addresses and data during free run mode:

Stimulus: free running			Timing pod	Polarity	Threshold
		1 2 3 4 5 6 7 8 9 10	Start: 90 TP ROM i	⎍	TTL
Test switch	on	x	Stop: 90 TP ROM i	⎍	TTL
	off	x x x	Clock: 90 TP $\overline{\text{OE}}$	⎍	TTL
High signature: P 2 5 4			Qual.: -	⎍	

i = 0 ... 5

A 0	5 P 3 3
A 1	F A 1 1
A 2	3 H U A
A 4	C 7 A 5
A 5	4 6 H C
A 6	6 5 C A
A 7	8 A U C
A 8	9 2 4 1
A 9	1 U 5 P
A 10	A A H U
A 11	U 6 6 5
A 12	8 2 6 P
A 13, A 14, A 15	0 0 0 0 or P 2 5 4 depending on address block connected

Table 7-4 Free run mode address signatures, ROM

The software-dependent signatures DØ ... D7 of the ROM data are determined in the same manner and compared with the signatures in the device.

7.4.3 RAM TEST

	1	2	3	4	5	6	7	8	9	10	
Switch 90 S 1	x	x	x		x	x	x	x		x	ON
				x					x		OFF

This routine tests the following:

- Immovable address lines
- Connections between address lines
- Internal and external RAM address decoders
- Memory location interlinks
- Correct writeability of storage cells with delay between writing and reading.

If an error is detected, the SOD signal remains at one logic level. The signatures of the address lines must then be checked. Refer to Section 7.4.2 for information on connecting and setting the signature analyzer.

$\overline{A\ 0}$	C F 6 7
$\overline{A\ 1}$	2 8 4 5
$\overline{A\ 2}$	H U A P
$\overline{A\ 3}$	U 0 A 4
$\overline{A\ 4}$	5 5 U 1
$\overline{A\ 5}$	A 4 8 U
$\overline{A\ 6}$	8 7 P P
$\overline{A\ 7}$	6 8 A U
$\overline{A\ 8}$	7 0 1 5
$\overline{A\ 9}$	U H 0 A
$\overline{A\ 10}$	4 8 8 C

Table 7-5 Free run mode address signatures, RAM

7.4.4 I/O TEST OF THE CPU BOARD

	1	2	3	4	5	6	7	8	9	10	
Switch 90 S 1	x	x		x	x	x	x	x		x	ON
			x						x		OFF

The test routine blocks the I/O strobe signals $\overline{RD}$, $\overline{WR}$ and $\overline{LSS}$ (HIGH), preventing activation of the I/O peripherals on the control board. The I/O addresses are then incremented and the same values output and reloaded on the I/O data bus. Correct functioning of the I/O data bus is thus tested.

If an error is detected, the SOD signal 90 IC 41.4 remains at one logic level. Refer to Section 7.4.5 for information on eliminating errors.

7.4.5 I/O TEST OF THE CONTROL BOARD

	1	2	3	4	5	6	7	8	9	10	
Switch 90 S 1			x	x		x	x	x		x	ON
	x	x			x				x		OFF

Unplug 6a, 17g, 7 and 17h on the board rack for the test!

The test routine addresses all output gates, input gates and D/A converters used. Different test patterns are written to the output gates. The test routine is used exclusively for signature analysis testing in two areas:

- PORT 1 for write signals
- PORT 2 for read signals

Go signatures:

Stimulus: PORT 1			Timing Pod	Polarity	Threshold
		1 2 3 4 5 6 7 8 9 10	Start: TP 212	⌐‾_	CMOS 5 V
Test	on	x x x x x x x	Stop: TP 212	_/‾_	CMOS 5 V
switch	off	x x x x	Clock: TP 204	⌐‾_	CMOS 5 V
High signature: A C C 4			Qual.: -	‾_	-

	Series D, E	Series F ...
IC 201.14	7 0 A P	7 0 A P
IC 205.2	9 H U 9	9 H U 9
IC 205.5	8 8 C H	8 8 C H
IC 205.6		F 6 H C
IC 205.7	F 6 H C	
IC 205.9		H 3 9 U
IC 205.10	H 3 9 U	
IC 205.11		8 6 6 5
IC 205.12	8 6 6 5	
IC 205.15	9 3 2 1	9 3 2 1
Comb		
7 c	9 A 7 3	9 A 7 3
8 c	3 8 H C	3 8 H C
9 c	1 1 1 7	1 1 1 7
10 c	6 5 9 1	6 5 9 1
11 c	2 0 F 0	2 0 F 0
12 c	3 4 P 7	3 4 P 7
13 c	2 2 2 U	2 2 2 U
14 c	6 7 7 P	6 7 7 P
15 c	1 A 6 U	1 A 6 U
16 c	9 0 F H	9 0 F H
17 c	3 7 U P	3 7 U P
18 c	C H 5 F	C H 5 F
19 c	6 9 F U	6 9 F U
20 c	P 3 6 H	P 3 6 H
21 c	4 4 5 P	4 4 5 P
22 c	F P U F	F P U F

Table 7-6 Signatures for "Go" testing of the control board [916-BP]: Port 1

Stimulus: PORT 2			Timing Pod	Polarity	Threshold
		1 2 3 4 5 6 7 8 9 10	Start: TP 212	⌐‾_	CMOS 5 V
Test	on	x x x x x x x	Stop: TP 212	_/‾_	CMOS 5 V
Switch	off	x x x x	Clock: TP 203	⌐‾_	CMOS 5 V
High signature: 0 0 U P			Qual.: -	‾_	-

	Series D ...
IC 228.1	0 0 C P
IC 229.1	0 0 7 U
IC 230.1	0 0 P P
IC 236.15	0 0 U 6

Table 7-7 Signatures for "Go" testing of the control board [916-BP]: Port 2

7.4.6 IEC INTERFACE

	1 2 3 4 5 6 7 8 9 10	
Switch 90 S 1	x x x x x x	ON
	x x x x	OFF

This routine tests whether the microprocessor can address and read the IEC interface. If not, the SOD signal 90 IC 41.4 remains at one logic level.

This is the only troubleshooting routine specifically for the optional standard assembly BN 958. If an error is localized in the interface assembly, it is generally sent to the manufacturer for repair.

7.5 TROUBLESHOOTING THE ANALOG SECTION

7.5.1 CHECKING THE SUPPLY VOLTAGES

The supply voltages are tested against 0 V on the board rack.

Test equipment required:
Digital voltmeter e.g. 8085A from Fluke

Supply voltage	Test point
+12 V $\pm$ 60 mV	17 pt 107
-12 V $\pm$ 60 mV	17 pt 109
+5 V $\pm$ 25 mV	17 pt 108

The AC voltage is measured off ground instead of against 0 V.
V_{rms} = 24 V $\pm$ 3 V 17 pt 101, 17 pt 102

7.5.2 TROUBLESHOOTING THE BB SECTION

At the BB section is troubleshooted to locate faults in the deflection voltage or test signal paths.

Test equipment required:
1 oscilloscope with 10 : 1 probe e.g. PM 3240 from Philips
PM 9350
1 frequency counter e.g. 1912 A from Fluke

7.5.2.1 Troubleshooting the deflection voltage signal path ($\hat{U}_A$)

Presettings on the RMS-5:

Deflection voltage	$\hat{U}_A$ [10] [2]	: 3.000 V
Deviation reduction	[5]	: OFF
Test voltage	U_M [13] [2]	: 0.0 mV

Checks (Series D, E)	Diagnosis and countermeasures if check negative
Voltage at (9) IC 101.7 = 10 V_{pp}	Wien bridge defective
Voltage at (9) IC 101.8 = 8.33 V_{pp}	Switch IC 106/3 or IC 101/2 defective
Voltage at (9) 24a = 8.33 V_{pp}	Check D/A converter using test routine
Voltage at emitter (16) T_1, (16) T_2 = 12 V_{pp}	Amplifier (16) IC 1 defective
Voltage at (16) pt 41 = 6 V_{pp}	Output filter defective
Voltage at jack Bu 5 = 6 V_{pp}	Cable or jack defective
Checks (Series F ...)	**Diagnosis and countermeasures if check negative**
(9) IC 104.14 f = 100 Hz or 120 Hz	Check clock frequency and/or line frequency conditioning
(9) IC 104.4 f = 4800 x f_A	PLL defective
(9) IC 107.9 f = 96 x f_A	Divider defective
(9) IC 111.7 $\hat{U}_A$ = 4.16 V_p at 18 Hz $\hat{U}_A$ = 4.32 V_p at 70 Hz	Divider or filter defective
Pt (9) 24a $\hat{U}_A$ = 8.33 V_{pp}	D/A converter or filter defective
Voltage at emitter (16) T_1, (16) T_2 = 12 V_{pp}	Amplifier (16) IC1 defective
Voltage at (16) pt 41 = 6 V_{pp}	Output filter defective
Voltage at jack Bu 5 = 6 V_{pp}	Cable or jack defective

7.5.2.2 Errors due to defective blanking intervals

The blanking interval is used to recognize and set the phase relationships for baseband distortion measurements in the receiver of the RME-5.

When the gap (6) has been activated, a gap pulse (9) 25c briefly reduces the test voltage in assembly (15), the U_M control element. The reducing pulse coincides in time with the positive peak of deflection voltage $\hat{U}_A$.

The U_M amplitude is only reduced very slightly and so difficult to see on the oscilloscope.

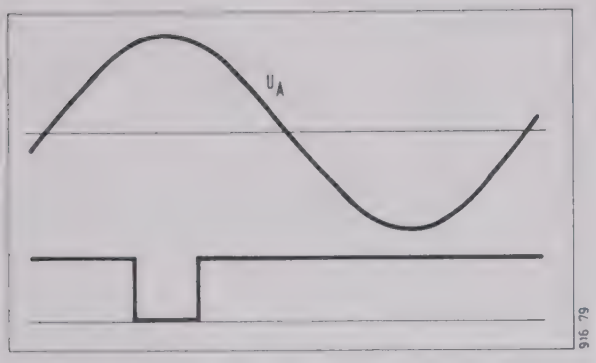


Fig. 7-9 Gap pulse

7.5.2.3 Troubleshooting the test signal path (U_M)

Presettings on the RMS-5:

Deflection voltage	[10]	: 0
Test voltage	U_M [13] [2]	: 500 mV
Test frequency	f_m [4]	: Set to maximum test frequency

Checks	Diagnosis and countermeasures if check negative
Voltage at (14) TP 2 = 3.5 V_{pp}	Test-frequency oscillator 2 defective
Voltage at (14) pt 71 = 1.3 V_{pp}	Divider chain or selector defective
DC voltage at (15) pt 63 = 4.56 V	Control voltage U_M incorrect
Voltage at (15) pt 64 = 470 mV_{pp}	U_M control element defective
Voltage at (15) TP 2 = 3 V_{pp}	U_M selection defective
Voltage at (15) pt 36 = 2.83 V_{pp}	U_M amplifier defective
Voltage at jack Bu 5 = 1.41 V_{pp}	Output filter (16) defective

Presettings on the RMS-5:

Test frequency	f_m [4]	: Set to minimum test frequency

Checks	Diagnosis and countermeasures if check negative
Voltage at (14) TP 1 = 3.5 V_{pp} Frequency at (14) TP 1 = 10 MHz	Test-frequency oscillator 1 or operating voltage filter defective

7.5.3 TROUBLESHOOTING THE IF SECTION

Defects in the IF section of the RMS-5 result in two types of error:

1. Level errors
2. Frequency errors - centre frequency, sweep width, test signal deviation

A frequency error, however, may also be caused by a fault in the level control circuit. An error in the centre frequency control can similarly give rise to sweep width errors. This is due to the fact that the various level circuits have sections in common. Troubleshooting starts with the frequency control circuit, since the IF frequency should be correct when testing the level control circuit.

Measuring equipment required:

1 DC power supply (up to 20 V)	e.g. 7730	Toellner
1 frequency counter (up to 250 MHz)	e.g. 1912A	Fluke
1 digital voltmeter	e.g. 8050A	Fluke
1 millivoltmeter with VHF probe	e.g. 411 A with probe 11023 A	hp
1 spectrum analyzer	e.g. 8558 B/182 T	hp
1 oscilloscope with 10 : 1 probe	e.g. PM 3240 with probe PM 9350	Philips

Instrument settings:

IF level	P_{IF} [8] [2]	: 0 dBm
IF centre frequency	[9] [2]	: 70 MHz
Sweep width	$\Delta\hat{F}$ [10]	: 0
Test deviation	Δf [13] [2]	: 0
External deflection voltage	$\hat{U}_{A\ EXT}$ [11]	: OFF
External test signal	U_M [12]	: OFF
Wideband option	[18]	: OFF

7.5.3.1 Troubleshooting the open frequency control circuit

The frequency control circuit comprises the following:
Frequency regulator: cannot be tested alone on account of integrator 9 IC 4
Oscillator section: sweep oscillator, modulation oscillator, mixer, pre-amplifier, frequency divider, discriminator.

Disconnect 9 TP 4 - 9 TP 5.

Checks	Diagnosis and countermeasures if check negative
1. DC voltage at 9 TP 7 = 0 V ± 50 mV f_{IF} at jack Bu [1] = 70 MHz ± 0.5 MHz Open connection St/Bu (17) f on the board rack	Frequency control circuit disconnected because of a defect
2. IF frequency at jack Bu (7) between 0 and 20 MHz	A defect in the oscillator area is likely if no signal is present or the frequency is very much higher.
3. Frequency IFD at 8 pt 74 and 8 pt 84 f = f_{IF}: 200	Frequency divider defective

Relationship between control voltage, oscillator and IF frequency:

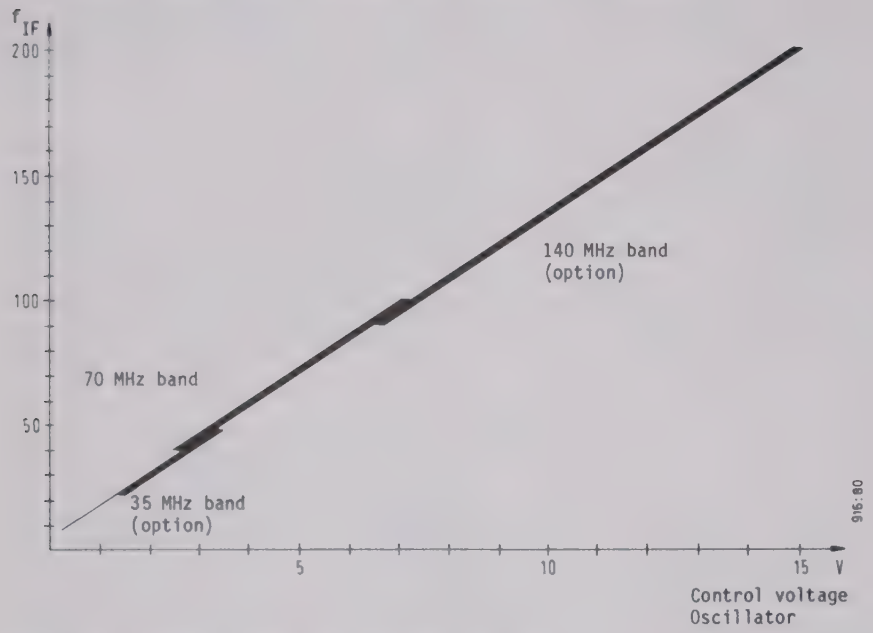


Fig. 7-10 Control voltage for the sweep oscillator

This relationship can be verified by applying a DC voltage to jack Bu (17) f and checking the frequency at jack Bu [7].

The divided frequency IFD can be measured at (8) jack 2 as follows:

Division ratio	35 MHz band	T = 1 : 100
	70 MHz band	T = 1 : 200
	140 MHz band	T = 1 : 400

depending on the set centre frequency (and possibly the sweep width).

The 70 MHz band is used with preference in areas where the bands overlap.

Relationship between IF frequency, divided IF frequency IFD and discriminator output voltage:

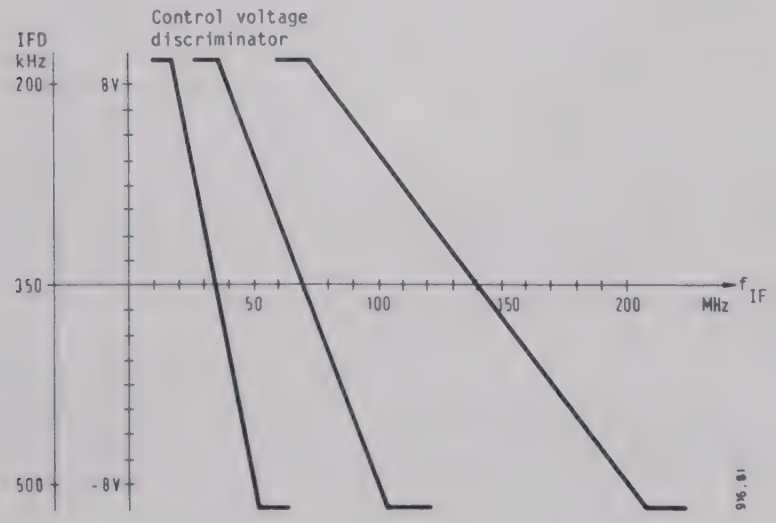


Fig. 7-11 Discriminator characteristics (8)

7.5.3.2 Troubleshooting the closed (operational) frequency control circuit

This procedure applies to errors in the sweep width setting, bandwidth limits, centre frequency control and frequency control linearity.

Checks	Diagnosis and countermeasures if checks negative
1. 9 TP 8: $f = 1/2\ f_A$	Check U_A generation
2. Check centre frequency control using test routine: bridge 9 TP 206 - 9 TP 207 Display: 10.00	Display 10.01: check centre frequency control assembly using signature analysis
3. Check D/A converter for centre frequency and $\Delta\hat{F}$ using test routine	Troubleshooting in control section
4. Check frequency control linearity using test routine; reconnect 9 TP 2 - 9 TP 3 and 9 TP 5 - 9 TP 6: Nominal display: 12.0	Amplifier 9 IC 3 defective

7.5.3.3 Troubleshooting level errors

Level errors are best localized and corrected on the basis of the following level schedule.

Presettings on the RMS-5:

IF level	P_{IF}	[8] [2]	: +10 dBm
IF centre frequency		[9] [2]	: 70.0 MHz
Sweep width	$\Delta\hat{F}$	[10]	: 0
Test deviation	Δf	[13] [2]	: 0
External deflection voltage	$\Delta\hat{U}_{A\ EXT}$	[11]	: OFF
External test signal	$U_{M\ EXT}$	[12]	: OFF
Wideband option		[18]	: OFF

Checks	Diagnosis and countermeasures if checks negative
1. Voltages at 12 pt 24: V_{rms} = 414 mV	Check level reference and D/A converter in (9)
2. Voltages at 5 pt 57: V = -5 V	Check DC voltage reference and D/A converter in (9)
3. Does the level at jack Bu [7] reflect the same level error?	The fault lies in the pre-amplifier before the branch, in the oscillator section or in the detector

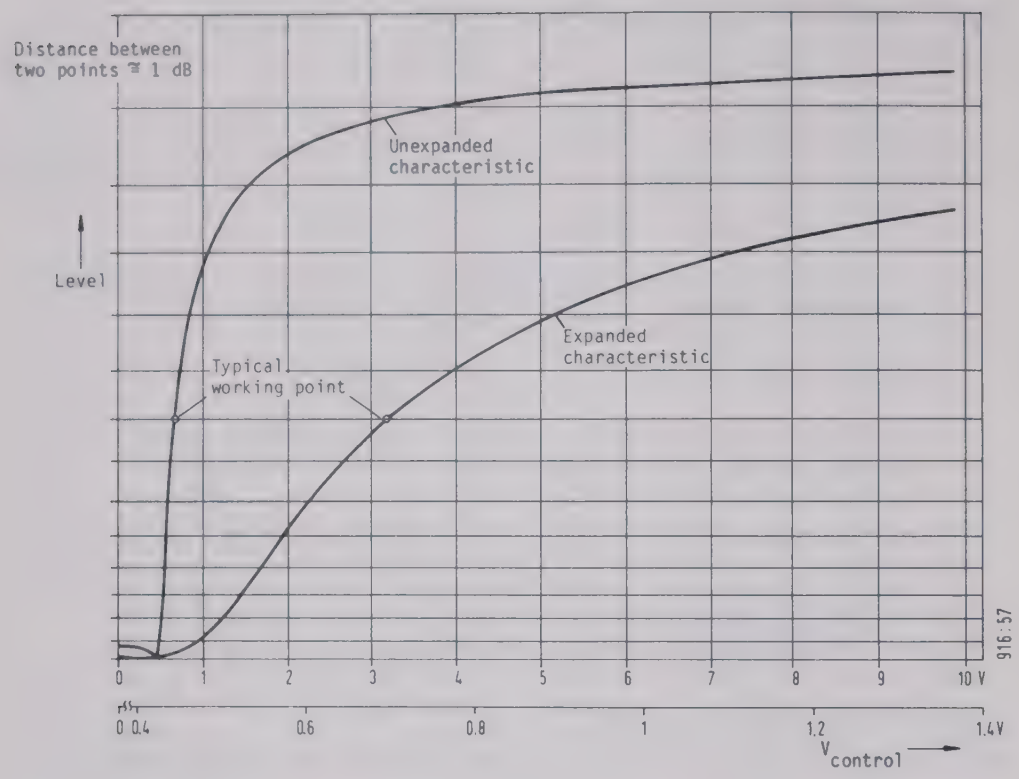
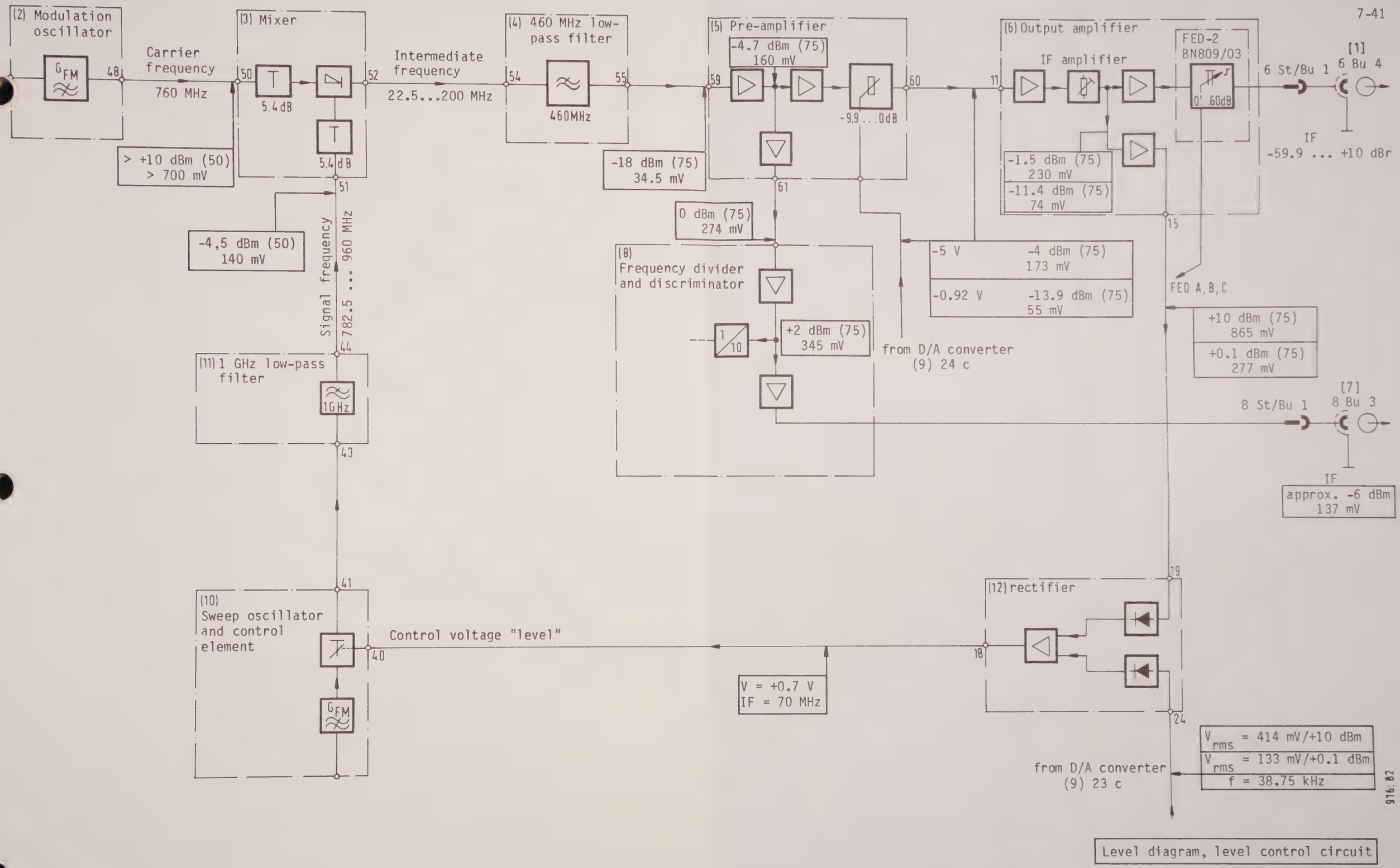


Fig. 7-12 Characteristic of the control element in the sweep oscillator (10)



Level diagram, level control circuit

Fig. 7-13 Level diagram of the IF section

7.6 MISCELLANEOUS TROUBLESHOOTING

Not applicable.

7.7 ALIGNMENT INSTRUCTIONS

This Section contains information on the alignments required when repairs are carried out on the RMS-5 or if the specified error limits are exceeded when verifying the technical data as described in Section 8.

Unless stated otherwise, the alignments should be carried out at room temperature (+23 °C ± 3 °C) after a warm-up period of 30 minutes.

Note: The screening covers should remain in position over the printed circuits where possible. The alignment elements are generally accessible via holes in the screening boxes, frames and covers.

7.7.1 OVERVIEW OF ALIGNMENTS

Trimmer	Alignment BN 844	Section
2 P 1	Supply voltage	7.7.2
2 P 3	Supply voltage	7.7.2
2 P 4	Supply voltage	7.7.2
Trimmer	**Alignment BN 916**	**Section**
2 C 5		-
2 C 8	Modulation oscillator	-
2 P 1		-
3 C 5	Mixer	-
3 C 6		-
5 C 31	Distortions	-
5 C 48	Frequency response P_{II}	-
5 P 31	IF linearity control element	7.7.5.3
5 P 32	Level P_{II}	7.7.5.2
5 P 33	IF offset control element (from series F)	7.7.5.3
6 C 13	Reflection coefficient P_I	-
6 C 14	Frequency response P_I	-
6 L 1	Reflection coefficient P_I	-
6 L 2	Frequency response P_I	-
6 L 17	Reflection coefficient P_I	-
6 P 1	IF amplification	7.7.5.3
8 C 7	Reflection coefficient P_{II}	-
8 P 41	Discriminator balance	7.7.4.3
9 L 1	Attenuation turning point 26.3 kHz	-
9 O 201	Level reference frequency	-
9 P 1	Frequency control linearity (linearity $U_{A\ EXT}$)	7.7.4.1

Table 7-8 Alignments

Trimmer	Alignment BN 916	Section
9 P 2		-
9 P 3	Control-voltage oscillator limiting (from Series F)	-
9 P 102	Deflection voltage, sweep width	7.7.4.2
10 C 4		-
10 C 5		-
12 L 1		-
12 P 1	IF level P_I	7.7.5.1
12 P 3		-
14 C 7	Amplitude for optional test frequency	7.7.3.1
14 C 13	Amplitude for optional test frequency	7.7.3.1
14 C 18	Frequency for optional test frequency	7.7.3.1
14 C 20	Frequency for test frequencies under 1 MHz	7.7.3.1
14 C 22	Frequency for optional test frequency	7.7.3.1
15 C 12	Test voltage amplitude	7.7.3.2
15 C 12	Test voltage amplitude	7.7.3.2
15 C 15	Test voltage amplitude	7.7.3.2
15 L 2	Test voltage amplitude	7.7.3.2
15 L 3	Test voltage amplitude	7.7.3.2
15 L 7	Test voltage amplitude	7.7.3.2
15 L 8	Test voltage amplitude	7.7.3.2
15 L 9	Test voltage amplitude	7.7.3.2
15 P 3	Test voltage amplitude	7.7.3.2
15 P 4	Test voltage amplitude	7.7.3.2
15 P 5	Test voltage amplitude	7.7.3.2
15 P 6	Test voltage amplitude	7.7.3.2
15 P 7	Test voltage amplitude	7.7.3.2
15 P 8	Test voltage amplitude	7.7.3.2
15 P 101	Amplitude U_M: -20 dB	7.7.3.3
15 P 102	Output level U_M	7.7.3.2
16 C 11	760 MHz residue	-
16 L 1 } 16 L 2 }	Output filter	- -
16 P 1	Modulation linearity	7.7.6
16 P 2	Modulation frequency response	-

Trimmer	Alignment Option 916/00.20	Section
18 L 1	Oscillating condition 140 MHz	-
18 L 2	Selection 140 MHz	-
18 L 3	Oscillating condition 70 MHz	-
18 L 4	Selection 70 MHz	-
18 L 5	Oscillating condition 35 MHz	-
18 L 6	Selection 35 MHz	-
18 P 1	Output level 140 MHz	-
18 P 2	Output level 70 MHz	-
18 P 3	Output level 35 MHz	-
18 C 31	Reflection coefficient	-

Table 7-8 Alignments (cont.)

7.7.2 ALIGNING THE SUPPLY VOLTAGES

Test equipment required:

1 digital voltmeter	e.g. 8085A	Fluke

The DC supply voltages are measured on the board rack and set via the control boards of the power supply unit BN 844.

Supply voltage	Test point	Alignment via
+12 V ± 60 mV	17 pt 107	2 P 3, BN 844
-12 V ± 60 mV	17 pt 109	2 P 4, BN 844
+5 V ± 25 mV	17 pt 108	2 P 1, BN 844

7.7.3 ALIGNMENTS IN THE BB SECTION

7.7.3.1 Aligning the test frequencies

Test equipment required:

1 oscillator with 10 : 1 probe	e.g. PM 3240 PM 9350	Philips
1 frequency counter	e.g. 1912A	Fluke

RMS-5:

Test voltage	U_M [13] [2]	: 0 dBm
Deflection voltage	$\hat{U}_A$ [10]	: 0

Oscilloscope:

Vertical resolution	: 0.5 V/div. (incl. probe)
Time-base deflection	: 50 ns/div.

Aligning the lower test frequencies (under 1 MHz)

- The three lower test frequencies are derived from an oscillator, the frequency of which is measured and set directly: connect the frequency counter to test point 14 TP 1 on the test frequency generator board [916-BX] or [916-BY] and adjust the frequency to (10)000.000 kHz ± 20 Hz using trimmer 14 C 20.

Aligning the higher test frequencies (over 1 MHz)

- Connect the frequency counter to output [17] (16 Bu 5) and the oscilloscope to 14 TP 2 on board [916-BX] or [916-BY] via the probe; align the amplitude maximum and the frequency as stated in Table 7-9; the required test frequency is activated via button [4]. The lower test frequency must always be aligned via 14 C 7 (amplitude) and 14 C 18 (frequency). The higher test frequency is then aligned via 14 C 13 (amplitude) and 14 C 22 (frequency).

f_m frequency (kHz)	permissible deviation [Hz]
2400.000	± 5
3580.000 *	± 7
3579.545 *	± 7
4430.000 *	± 7
4433.619 *	± 7
5600.000	± 11

Table 7-9 Alignment of the test frequencies over 1 MHz

7.7.3.2 Aligning test voltage U_M

Test equipment required:

1 calibrated level meter with probe e.g. EPM-1 W&G

RMS-5:

Test signal level	U_M [13] [2]	: 0 dBm
Deflection voltage	$\hat{U}_A$ [10]	: 0
Test frequency	f_m [4]	: 83.3 kHz
		92.6 kHz

EPM-1:

Measuring range		: ± 0.2 dBm
Output impedance	Z_{out}	: 75 ohm
Calibration level		: 0 dBm

Connect probe of EPM-1 to jack BU [17].

- Using 15 L 9, set the output level on board U_M amplifier [916-BZ] or [916-CA] to maximum and then adjust to 0.0 dBm ± 0.04 dB on board U_M control element [916-BO] using 15 P 102.
- For the frequencies listed in Table 7-10, first determine the maximum level and set the frequencies of the oscillating circuit using 15 L ... or 15 C ... and then set the level using 15 P ....

f_m No.	1	2	4	5	6	7
L or C	15 L 2	15 L 3	15 L 8	15 L 7	15 C 12	15 C 15
Pot	15 P 3	15 P 4	15 P 8	15 P 7	15 P 5	15 P 6

Nominal value: 0.0 dBm Alignment tolerance: ± 0.04 dB

Table 7-10 Aligning the test voltage

* = Option

7.7.3.3 Aligning the 20 dB divider "U_{M20}"

Test equipment required:

1 20 dB attenuator pad	BN 920/20	W&G
1 RME-5	BN 917	W&G

RM-5:
BB measurement
RMS-5:

Deflection voltage	$\hat{U}_A$	[10]	: 0
Test voltage	U_M	[13] [2]	: 0 dBm
Test frequency	f_M	[4]	: 250 kHz 277 kHz

RME-5:

Mode "BB level"		[28]	: ON

Connect jack Bu [17] (U_A + U_M) of the RMS-5 with jack Bu [29] of the RME-5 by inserting the 20 dB attenuator pad.
Remember or note the BB level displayed.

Setting on the RMS-5:

Test signal	U_M	[13]	: -20 dBm

Remove attenuator pad!

The new BB level displayed must be adjusted to the value measured before ± 0.01 dB: alignment via 15 P 101.

7.7.4 ALIGNING THE CONTROL BOARD

7.7.4.1 Aligning frequency control linearity

This alignment is performed using a test routine:

Test routine	1	2	3	4	5	6	7	8	9	10	
	x		x			x	x	x		x	ON
		x		x	x				x		OFF
Normal operation	x	x	x	x		x	x	x		x	ON
f_m series I					x				x		OFF
Normal operation		x	x	x		x	x	x		x	ON
f_m series II	x				x				x		OFF

Switch 90 S 1

Connect: 9 TP 2 - 9 TP 3 and 9 TP 5 - 9 TP 6. Switch on the device again.
A value of approximately 12 appears on each of the three left-hand displays after a short delay.

Adjust the centre display to 12.00 ± 0.02 using 9 P 1.

Restore the original status of the wire links and switch 90 S 1.

7.7.4.2 Aligning the sweep width $\Delta\hat{F}$ and deflection voltage $\hat{U}_A$

This alignment must be preceded by a check or alignment as described in Section 7.7.4.1.

Equipment required:
1 RME-5 W&G

RM-5:
IF measurement
RMS-5:

IF level	P_{IF} [8] [2]	: 0 dBm
IF centre frequency	[9] [2]	: 70 MHz
Sweep width	$\Delta\hat{F}$ [10] [2]	: 9.90 MHz
Deflection frequency	f_A [14]	: 18 Hz

RME-5:

IF mode	[22]	: ON
IF centre frequency	[21]	: 70 MHz

Connect jack Bu [1] on the RMS-5 with jack Bu [25] on the RME-5.
Using 9 P 102 on the RMS-5, set the display for $\Delta\hat{F}$ to 9.90 MHz on the RME-5.

7.7.4.3 Aligning the discriminator balance

This alignment is required on account of the small range reserves of the centre frequency control. If the discriminator is not balanced, the limit areas of the IF bandwidths cannot be attained and/or cut off results when sweeping, this in turn displaces the centre frequency.

Test equipment required:
1 digital voltmeter e.g. 8050A Fluke

IF centre frequency	[9] [2]	: 70.0 MHz
Sweep width	[10]	: ON
Wideband option	[18]	: OFF

Using 8 P 41, align the DC voltage at 9 TP 4 until it equals 0 V $\pm$ 50 mV.

7.7.5 ALIGNING THE IF SECTION

7.7.5.1 Aligning the IF output level P_I (Bu [1])

Test equipment required:
1 calibrated level meter e.g. EPM-1 W&G

RMS-5:

IF level	P_I [8] [2]	: 0 dBm
IF centre frequency	[9] [2]	: 70.0 MHz
Sweep width	$\Delta\hat{F}$ [10]	: 0

Connect the probe of the EPM-1 with jack Bu [1]. Calibrate the EPM-1 with 0 dBm, Z_{in} = 75 Ω.
Using 12 P 1, adjust the output level to 0 dBm $\pm$ 0.02 dB.

7.7.5.2 Aligning the IF output level P_{II} (Bu [7])

This alignment is required whenever a defect is found in the P_{II} IF path between the branch point in the 200 MHz amplifier (5) and jack Bu [7].

Test equipment required:
1 RME-5

RM-5:
IF measurement
RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: 70 MHz
Sweep width	$\Delta\hat{F}$	[10]	: 0
Wideband option		[18]	: OFF
RME-5:			
Mode "IF counter"		[4]	: ON
IF centre frequency		[21]	: 70 MHz

Connect jack Bu [7] on the RMS-5 with jack Bu [25] on the RME-5.
Adjust the transmission level P_{IF} [8] on the RMS-5 in steps of +0.1 dBm, +5 dBm, +10 dBm and set 5 P 32 on the RMS-5 so that -6 dBm is measured on average on the RME-5.

7.7.5.3 Level alignment in the IF path

This alignment concerns both 5 P 31 and 6 P 1 (and 5 P 33 from series F).

These potentiometers are set by the manufacturer using special test equipment and must satisfy a number of requirements:

- Maximum gain in the P_I IF path = 30 dB (28 dB from series F).
- The change in gain must be as nearly 9.9 dB when
- The control voltage is adjusted from -5 V to -0.9 V.
- The level control voltage at 12 pt 18 must be virtually constant at approx. 0.7 V.
- There must be no distortion changes due to level changes when using the highest test frequency.

7.7.6 ALIGNING THE TEST SIGNAL DEVIATION Δf

Test equipment required:
1 RME-5 W&G

RM-5:
IF measurement
RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: 70 MHz
Sweep width	$\Delta\hat{F}$	[10]	: 0
Test frequency	f_m	[4]	: 250 kHz 277 kHz

RME-5:

"Bessel zero" mode	[3]	: ON
IF centre frequency	[21]	: 70 MHz

Connect jack Bu [1] on the RMS-5 with jack Bu [25] on the RME-5.

f_M	Δf	U_M
250 kHz	425 kHz	3.82 dBm, 425 mV
277 kHz	472 kHz	7.74 dBm, 472 mV

Table 7-11 Relationship between Δf and U_M for calibration test frequencies

Δf [13] is set on the RMS-5 in accordance with the available test frequency.

Align 16 P 1 in the RMS-5 so that the middle line in the Bessel spectrum is a minimum. In case of doubt, check U_M at jack Bu [17] after setting the U_M value via [13].

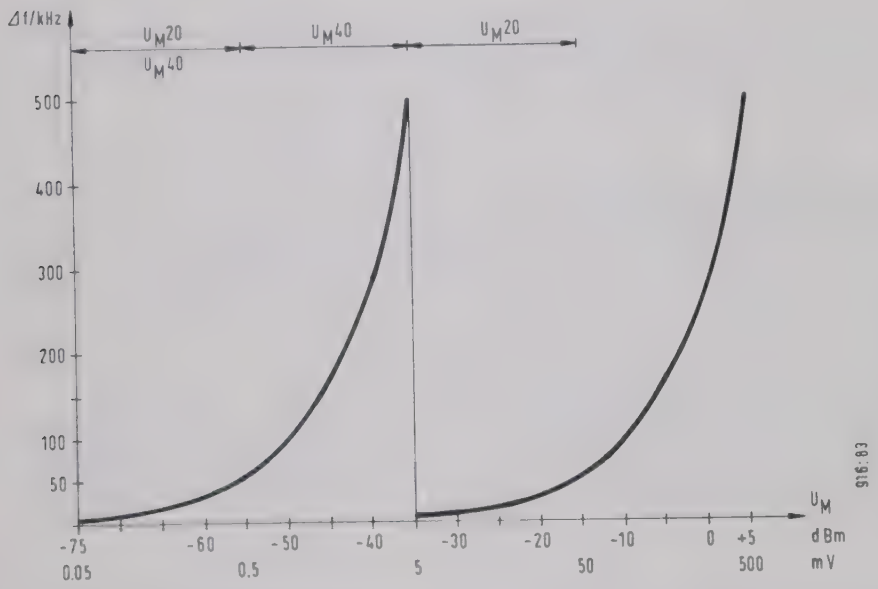


Fig. 7-14 Relationship between U_M and Δf

8 VERIFICATION OF TECHNICAL DATA

8.1 INTRODUCTION

This section describes methods by which the technical data of the unit can be verified. Commercially available test instruments have been recommended wherever possible. It is presumed that the unit is fully operational at the time of testing.

Unless stated otherwise, the tests and possible adjustments should be performed within the specified nominal service temperature range and after the appropriate warm-up period.

The technical data are verified in order to ascertain whether the measured value displayed or output lies within the specified error limits. This can only be ascertained correctly if the inherent error of the test set-up used is negligible. An additional method using in-house test instruments and headed "In-house test" is given for those cases where commercially available test instruments cause significant errors in the test set-up.

When deciding whether errors lie within the specified limits, the error caused by the test set-up is attributed to the test equipment (IEC Publication 359).

This principle can be explained on the basis of symmetrical error limits, for example. If the error limit for the test set-up used is $\pm$ m and the specified error limit for the specimen is $\pm$ e, then the following applies:

If the limits $\pm$ (e + m) are exceeded,
this proves that the specified error limits
have definitely been exceeded.

If the limits $\pm$ (e - m) are not reached,
this proves that the specified error limits
have definitely been observed.

Values for e and m are given for each test method, insofar as they are required. Value m depends on the test instrument used and must, therefore, be re-determined when deviating from the test instructions.

We recommend that the tests be performed in the order stated when systematically verifying the technical data.

Note: Verification of the technical data of the RM-5 measuring setup as a whole is described in Section 8 of the RME-5 Service Manual; verification of the "wideband modulator" is described in Section 8 of the RMED-5 Service Manual.

8.2 FREQUENCIES

Test equipment required:

1 frequency counter	1912A	Fluke

8.2.1 BB FREQUENCIES

Test frequencies:

RMS-5:

Deflection voltage	$\hat{U}_A$	[10]	: 0
Test voltage	U_M	[13] [2]	: over -10 dBm
Test frequency	f_m	[4]	: see Table 8-1

Connect the frequency counter to BB output $\hat{U}_A + U_M$ [17]. The internal test frequencies [4] are set and measured in accordance with the table below:

Test frequency (4)/kHz		Nominal value/kHz		Error limits (e)/kHz	
Series I	Series II	Series I	Series II	Series I	Series II
27	25	27.778	25.000	± 0.56	± 0.50
55	50	55.556	50.000	± 1.11	± 1.00
92	83	92.593	83.333	± 1.85	± 1.67
277	250	277.778	250.000	± 5.56	± 5.00
555	500	555.556	500.000	± 11.11	± 10.00
2400		2400.000		± 48.00	
3579		3579.545		± 71.59	
3580		3580.000		± 71.60	
4430		4430.000		± 88.60	
4433		4433.619		± 88.67	
5600		5600.000		± 112.00	

Table 8-1 Test frequencies

Test setup error (m): $5 \times 10^{-8} \times f_M \pm 0.1$ Hz

Deflection frequencies:

RMS-5:

Test voltage	U_M [13] [2]	: 0
Deflection voltage	$\hat{U}_A$ [10] [2]	: over 0.3 V
Deflection frequency	f_A [14]	: see table 8-2

Connect the frequency counter to BB output $\hat{U}_A + U_M$ [17]. Measure the period mean ($N = 10^2$) of the internal sweep frequencies [14] and compare with table 8-4.

Deflection frequency f_A [14]	Nominal value	Error limits (e)	Test setup error (m)
70 Hz	14.286 ms	± 0.286 ms	± 4.3 µs
18 Hz	55.556 ms	± 1.111 ms	± 16.7 µs
other (options)	$1/f_A$	$\pm 2 \times 10^{-2}/f_A$	$\pm 3 \times 10^{-5}/f_A$

Table 8-2 Deflection frequencies

8.2.2 IF FREQUENCIES

RMS-5:

IF level	P_I [8] [2]	: 0 dBm
IF centre frequency	[9] [2]	: see table 8-3
Sweep width	$\Delta\hat{F}$ [10]	: 0
Test tone deviation	Δf [13] [2]	: 0

Connect the counter to IF output (1). Settings and measurements as per the table below.

	35 MHz range (option)	70 MHz range	140 MHz range (option)
Frequency setting [2] [9]	22.5; 25; 30; 35; 40; 45; 47.5 MHz	40; 45; 58; 70; 82; 95; 100 MHz	90; 110; 122; 140; 158; 170; 190; 200 MHz
Error limits (e)	± 10 kHz	± 20 kHz	± 40 kHz

Table 8-3 IF frequencies

Test setup error (m): negligible (5×10^{-7})

Note: If the 35 MHz and/or 140 MHz options are installed, the lower error limits apply for the over lapping values.

Frequency of the IF calibration generator (option):

Connect the counter to the IF_0 output [15] and measure the frequency (frequencies).

Frequency setting [2] [9]	35 MHz (option)	70 MHz	140 MHz (option)
Error limits (e)	± 1.75 kHz	± 3.5 kHz	± 7 kHz

Table 8-4 IF_0 frequencies

8.3 LEVEL MEASUREMENTS

Test equipment required:

1 milliwatt power meter	EPM-1	BN 564/0	W&G
with accessories	TK-10	BN 572/0	W&G
1 attenuator pad 3 dB/75 Ω	DG-1403	BN 921/10	W&G
1 selective level meter	SPM-16	BN 874/xx	W&G
1 calibrated attenuator (Z_0 = 75 Ω)	D-2053		Siemens

8.3.1 BB LEVEL

RMS-5:

Deflection voltage	$\hat{U}_A$ [10]	: 0
Test voltage	U_M [13] [2]	: 0 dBm

EPM-1:

Measuring range		: ± 0.2 dBm
Output impedance	Z_{out}	: 75 Ω
Calibration level		: 0 dBm

SPM-1:

Display mode	[4]	: DGTL
Display averaging	[11]	: ON
AFC	[5]	: ON
Bandwidth	[16]	: ≤ 1.74 kHz

Test voltage U_M

Connect the probe of the EPM-1 to BB output [17] of the RMS-5. Activate the test frequencies (4) in succession and note the level deviation from 0 dBm in each case.

Error limits (e): ± 0.5 dB
Test setup error (m): ± 0.015 dB

Note: The above error limits for the test setup apply only for temperatures between 20 °C and 26 °C (otherwise (m): ± 0.035 dB).

Linearity

D-2035
Attenuation :75 dB

Connect the SPM-16 to BB output [17] via the D-2053. Find the reference value by subtracting the result of the preceding measurement (ΔL_{EPM-1} at 0 dBm) from the value displayed on the SPM-16 with the correct sign. Note the deviations for each test frequency and at various levels. Attenuation changes up to increments of 1 dB must be compensated on the attenuator set. Recommended level settings (in dBm):

U_M/dBm	+5.2	-14.5	-15	-25	-34.5	-35	-45	-54.5	-55	-65	-74.5
Error limits (e)	± 0.5 dB										
Test setup error (m)	± 0.04 dB										

Table 8-5 U_M linearity

Note: The above error limits for the test setup apply provided that only the 1 dB and 10 dB increments on the calibrated attenuator were altered during the measurement.

Deflection voltage $\hat{U}_A$

RMS-5:

Test voltage	U_M	[13] [2]	: 0
Deflection voltage	$\hat{U}_A$	[10]	: see text
Deviation reduction		[5]	: OFF

EPM-1:

Measuring range		: ± 0.2 dBm
Output impedance	Z_{out}	: 75 Ω
Calibration level		: 0 dBm

Connect the EPM-1 to BB output [17] via the D-2053. Settings and measurements as per the following table for both deflection frequencies [14].

Deflection voltage to be set $\hat{U}_A/mV_p$	500	1000	1500	2000	2500	3000
Nominal attenuation $(a_{cal} + \Delta L_{EPM-1})/dB$	2.22	8.24	11.76	14.26	16.20	17.78
Error limits (e)	$\pm$ 0.26 dB ($\pm$ 3%)					
Test setup error (m)	$\pm$ 0.06 dB					

Table 8-6 Deflection voltage $\hat{U}_A$

Note: The above error limits for the test setup apply only for temperatures between 20 °C and 26°C and for $a_{k3} \geq 46$ dB (typically: > 50 dB).

Sweep reduction

Set the deflection voltage to 2500 mV_p, activate the test voltage [13] (U_M < -70 dBm!) and measure the values as per the following Table with sweep reduction on. The error conditions outlined above are also applicable here.

Test frequency to be set f_M [4]/kHz	555 or 500	2400	3580 or 3579	4433 or 4430	5600
Nominal attenuation $(a_{cal} + \Delta L_{EPM-1})/dB$	16.00 or 16.03	15.32	14.86	14.50	14.00

Table 8-7 Sweep reduction

8.3.2 IF LEVEL

Absolute level and frequency response at L $\geq$ 0 dBm.

RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: 70 MHz
Sweep width	$\Delta\hat{F}$	[10]	: 0
Test tone deviation	Δf	[13] [2]	: 0

EPM-1:

Measuring range		: $\pm$ 0.2 dBm
Output impedance	Z_{out}	: 75 Ω
Calibration level		: 0 dBm

a) Absolute level of the IF output [1]

Connect the probe of the EPM-1 to IF master output [1]. Note the value displayed on the EPM-1. Repeat the measurements on the 35 MHz and/or 140 MHz options installed.

Frequency	35 MHz (option)	70 MHz	140 MHz (option)
Error limits (e)	± 0.15 dB	± 0.15 dB	± 0.25 dB
Test setup error (m)	± 0.015 dB	± 0.025 dB	± 0.040 dB

Table 8-8 Absolute level at 0 dBm

Note: The above error limits for the test setup apply only for temperatures between 20 °C and 26 °C (otherwise the values must be increased by 0.02 dB).

b) Frequency response of the IF output [1] at +3 dBm [8] [2]

Connect the EPM-1 to IF output [1] with upstream 3 dB attenuator pad. Incrementally adjust the centre frequency (in approx. 20 increments) and note any changes in the values displayed on the calibrating level meter. Note the highest and lowest values.

Frequency range	25 to 45 MHz (option)	40 to 100 MHz	90 to 200 MHz (option)
Error limits (e) (referred to the mean value)	± 0.05 dB	± 0.05 dB	± 0.1 dB
Test setup error (m)	± 0.032 dB	± 0.034 dB	± 0.05 dB

Table 8-9 Frequency response at +3 dBm

Note: The above error limits for the test setup apply only for temperatures between 20 °C and 26 °C and taking into account the intrinsic frequency response of the TK-10.

c) Frequency response of the IF output [1] at 0 and +9 dBm [8] [2]

Connect the EPM-1 to IF output [1] with or without the 9.03 dB attenuator pad (EPM-1 accessory) connected upstream. Then measure the values at the corresponding output levels as above.

Frequency range	25 to 45 MHz (option)	40 to 100 MHz	90 to 200 MHz (option)
Error limits (e)	± 0.1 dB	± 0.1 dB	± 0.3 dB
Test setup error (m) at 0 dBm	± 0.012 dB	± 0.017 dB	± 0.031 dB
Test setup error (m) at +9 dBm	± 0.016 dB	± 0.020 dB	± 0.043 dB

Table 8-10 Frequency response at 0 dBm and +9 dBm

Note: The above error limits for the test setup apply only for temperatures between 20 °C and 26 °C and taking into account the intrinsic frequency response of the TK-10.

d) Absolute level of the IF_0 output (option) [15]

Connect the EPM-1 to the IF_0 output [15] via the calibrated attenuator. Set the attenuation to 5 dB on the calibrated attenuator. Read off the value displayed on the EPM-1. Note any deviation from 0. Perform the measurement at 70 MHz and at 35 MHz and/or 140 MHz (if available).

Frequency	35 MHz (option)	70 MHz	140 MHz (option)
Error limits (e)	± 0.5 dB	± 0.5 dB	± 0.5 dB
Test setup error (m)	± 0.13 dB	± 0.14 dB	± 0.19 dB

Table 8-11 Absolute level of the IF_0 output

Divider error at IF main output [1]:

Connect the SPM-16 to IF output [1] via the calibrated attenuator.

SPM-16:

Display mode	[4]	: DGTL
Display averaging	[11]	: ON
Frequency	[7] [12]	: 70 MHz
AFC	[5]	: ON
Bandwidth	[16]	: 3.1 kHz

D-2053:

Attenuation		: 56 dB

Set the IF level to 0 dBm on the RMS-5. Determine the reference value by subtracting the absolute value measured with correct sign from the value displayed on the SPM-16. Determine the deviation from 0 of the value displayed on the SPM-16 by lowering the level on the unit under test and reducing the attenuation correspondingly on the calibrated attenuator. Compare the result with the error limits compiled in Table 8-12. Recommended measuring range: 0 to 55 dB in 5 dB increments. Repeat the measurement for the other centre frequencies installed.

Frequency	35 MHz (option)	70 MHz	140 MHz (option)
Error limits (e)	± 0.5 dB	± 0.5 dB	± 0.5 dB
Test setup error (m)	± 0.06 dB	± 0.06 dB	± 0.15 dB

Table 8-12: IF divider error

Note: The above error limits for the test setup apply provided that only the 1 dB and 10 dB stages are altered during the measurement.

8.4 D E V I A T I O N M E A S U R E M E N T S

Test equipment required:

1 spectrum analyzer	182T/8558B		hp
1 Matching pad 50/75 Ω	ZA 5075	BN 925/03	W&G
1 Receive section of RM-5	RME-5	BN 917/xx	W&G

8.4.1 TEST TONE DEVIATION Δf (RMS)

RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: 70 MHz
Sweep width	$\Delta\tilde{F}$	[10]	: 0

8558B (spectrum analyzer):

Frequency	: Centre, 70 MHz, calibrated	
Reference level	: approx. -4 dBm	
Optimum input	: 0 dBm	} coupled
Frequency span/division	: 50 kHz	} coupled
Resolution bandwidth	: 3 kHz	} coupled
Time/Div.	: ⋈Auto	
Trigger	: Free Run	
Resolution	: 10 dB/Div.	

Connect the spectrum analyzer to the IF output [1] of the RMS-5 via the matching pad. Activate $U_{M\ EXT}$ [12] on the RMS-5. Set the reference level on the analyzer so that the unmodulated carrier amplitude touches the reference line on the monitor; then switch off $U_{M\ EXT}$.

Carry out the measurements in accordance with the table below:
Set the table value Δf_{nom} on the RMS-5 [2], [13]. Note the residual carrier on the screen and minimize by precision adjustment of Δf (Bessel zeroes) if the carrier suppression is less than 50 dB. Note Δf_{actual} and determine the deviation from Δf_{nom}.

Error limits (e): $\pm$ 0.08 x Δf

Test setup error (m)

for Δf under 50 kHz: $\pm$ 0.2 kHz

for Δf = 50 kHz and more: $\pm$ 1 kHz

Nom. test deviation Δf_o (Bessel) / Carrier zero	Δf_{nom} for f_M							
	Series I 25 kHz	Series II 27.7 kHz	I 50 kHz	II 55.5 kHz	I 83.3 kHz	II 92.6 kHz	I 250 kHz	II 277 kHz
1	42.5	47.2	85	94.5	141.7	157.5	425.1	472.4
2	97.6	108.4	195.2	216.9	325.1	361.4		
3	153	170	306	340				
4	208.5	231.6	416.9	463.2				
5	264	293.3						
6	319.5	355						
7	375	416.6						
8	430.5	478.3						
9	486.1							

Table 8-13 Nominal test tone deviation Δf_o

Note: Recommended setting on the spectrum analyzer for freq. span/div.: $\frac{f/D}{f_M}$ = approx. 1
(e.g. for f_M = 92.6 kHz, f/D = 100 kHz/Div.)

8.4.2 SWEEP WIDTH $\Delta\hat{F}$

RM-5:
IF measurement

RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: see table 8-14
Sweep width	$\Delta\hat{F}$	[10] [2]	: see table 8-14
Test tone deviation	Δf	[13] [2]	: 0

RME-5:

IF mode	[22]	: ON
IF centre frequency	[21]	: see table 8-14
ΔP_I mode	[2]	: ON
Automatic level control	[30]	: ON

Make the IF connection between transmitter and receiver ([1]-[25]). Set the other parameters in accordance with the table below. Note the sweep width displayed ($\Delta\hat{F}$ on the lower edge of the screen) in each case and compare with the set value ($\Delta\hat{F}$ on the RMS-5).

IF centre frequency	35 MHz (option)	70 MHz		140 MHz (option)
Sweep width $\Delta\hat{F}$	12.5 MHz	9 MHz	30 MHz	50 MHz
Error limits (e)	$\pm$ 0.4 MHz	$\pm$ 0.30 MHz	$\pm$ 0.9 MHz	$\pm$ 1.5 MHz
Test setup error (m)	$\pm$ 0.16 MHz	$\pm$ 0.055 MHz	$\pm$ 0.25 MHz	$\pm$ 0.35 MHz

Table 8-14 Sweep width $\Delta\hat{F}$

Sweep reduction

Set a sweep width of 14.0 MHz [10] [2] for a centre frequency [9] of 70 MHz on the RMS-5. Switch on the deviation reduction [5] and select the highest test frequency f_M [4]. Note the sweep width $\Delta\hat{F}$ displayed on the RME-5 and compare with the nominal value.

Nominal value $\Delta\hat{F} = \pm (14.0 - f_M)$ MHz
Error limits (e): $\pm [0.03 \times (14.0 - f_M) + 0.03]$ MHz
Test setup error (m): $\pm [0.005 \times (14.0 - f_M) + 0.01]$ MHz

8.5 H A R M O N I C R A T I O S

Test equipment required:

1 spectrum analyzer	182T/8558B		hp
1 Matching pad 50/75 Ω	ZA-5075	BN 925/03	W&G
1 selective level meter	SPM-11	BN 604/xx	W&G

8.5.1 HARMONIC RATIO OF THE BB SIGNALS

Test voltage $\hat{U}_M$

RMS-5:

Deflection voltage	U_A	[10]	: 0
Test voltage	U_M	[13] [2]	: 500 mV
Test frequency	f_m	[4]	: see text

8558B (spectrum analyzer):

Optimum input	: 0 dBm
Freq. span/div.	: 2 MHz or $f_m/3$
Frequency	: Start 0 MHz calibrated
Resolution bandwidth	: 30 kHz or $f_m/15$
Time/div.	: ⋈ Auto
Trigger	: Free Run
Resolution	: 10 dB/div.

Measurement for f_M over 80 kHz

Connect the spectrum analyzer to the BB output [17] of the RMS-5 via the matching pad. Set the reference level on the analyzer so that the fundamental wave reaches the 0 dB line on the screen in each case. Then read off a_{k2} and a_{k3}. Repeat the measurement for all test frequencies [4] over 80 kHz selecting a suitable bandwidth ($B_{Res} \leq f_M/15$).

Specified limit value (e): a_{k2}, a_{k3}: $\geq$ 30 dB
Test setup error (m): $\pm$ 1.8 dB

Measurement for f_M less than 66 kHz

RMS-5:			
Deflection voltage	$\hat{U}_A$	[10]	: 0
Test voltage	U_M	[13] [2]	: 500 mV
Test frequency	f_m	[4]	: see text
SPM-11:			
Mode		[10]	: Log.
Measuring range		[3]	: 0 dB
Bandwidth		[6]	: 40 Hz

Connect input [8] of the SPM-11 with the BB output [17] of the RMS-5. Adjust the SPM-11 to the fundamental to be measured [7]. Set the reference value to the 0 dB scale value using the calibrating potentiometer [5] on the SPM-11. Then adjust to the first and second harmonics and read off a_{k2} and a_{k3}.

Specified limit value (e): a_{k2}, a_{k3}: $\geq$ 30 dB
Test setup error (m): $\pm$ 1.7 dB

Deflection voltage $\hat{U}_A$

RMS-5:			
Test voltage	U_M	[13] [2]	: 0
Deflection voltage	$\hat{U}_A$	[10] [2]	: 3 V
Deflection frequency	f_A	[14]	: see text
SPM-11:			
Mode		[10]	: Lin., low noise
Measuring range		[3]	: +10 dB
Bandwidth		[6]	: 8 Hz

Determine the reference value as described above. Adjust the SPM-11 to the first and second harmonics, increasing the sensitivity of the measuring range by 40 dB. Note a_{k2} and a_{k3}. Repeat the measurement for both deflection frequencies [14].

Specified limit value (e): a_{k2}, a_{k3}: $\geq$ 40 dB
Test setup error (m):
for f_A over 20 Hz, a_{k2} or a_{k3}: $\pm$ 0.5 dB
for f_A = 18 Hz, a_{k3}: $\pm$ 0.5 dB
for f_A = 18 Hz, a_{k2}: + 2.3/-3.1 dB

8.5.2 HARMONIC RATIO OF THE IF SIGNALS

RMS-5:

IF level	P_I [8] [2]	: see text
IF centre frequency	[9] [2]	: see text
Sweep width	$\Delta\hat{F}$ [10]	: 0
Test tone deviation	Δf [13] [2]	: 0

8558B (spectrum analyzer):

Optimum input	: as IF level
Freq. span/div.	: 10 MHz
Resolution bandwidth	: 100 kHz
Time/div.	: ⋈Auto
Trigger	: Free Run
Resolution	: 10 dB/div.

Connect the spectrum analyzer to the IF output [1] of the RMS-5 via the matching pad. Set the reference level on the spectrum analyzer so that the fundamental touches the 0 dB line on the screen in each case. Then adjust the spectrum analyzer to a_{k2} and a_{k3} and note the values displayed. Repeat the measurement for the +10 dBm and -10 dBm levels in the following frequency ranges:

for IF = 70 MHz	40 to 100 MHz
for IF = 35 MHz (option)	25 to 40 MHz
for IF = 140 MHz (option)	90 to 200 MHz

Also repeat the measurement at the IF_0 output [15] (if installed) for all installed IF centre frequencies.

Specified error limit (e): a_{k2}, a_{k3}: $\geq$ 30 dB
Test setup error (m): $\pm$ 1.8 dB

8.6 R E T U R N L O S S E S

Test equipment required:

1 receive section of RM-5	RME-5	BN 917	W&G
1 send section of RM-5	RMS-5	BN 916	W&G
1 selective level meter	SPM-16	BN 874	W&G
1 level generator (SPM-16 generator)	PSS-16	BN 873	W&G
1 return loss coefficient measuring bridge	RFZ-4	BN 697	W&G
1 return loss measuring attachment	RFZ-5	BN 394	W&G
1 digital multimeter	8050A		Fluke

8.6.1 RETURN LOSS OF THE BB CONNECTIONS

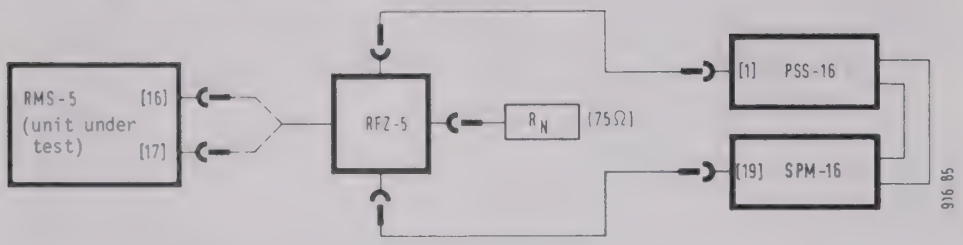


Fig. 8-1 Test setup for section 8.6.1

SPM-16:			
Display mode		[4]	: DGTL
Frequency		[7] [12]	: approx. 2 MHz, see text
Bandwidth		[16]	: 400 Hz
PSS-16:			
Level		[2]	: +10 dBm
RMS-5 (unit under test):			
Deflection voltage	$\hat{U}_A$	[10]	: 0
Test signal level	U_M	[13] [2]	: +5 dBm or -40 dBm
Test frequency	f_m	[4]	: 83.3 kHz 92.6 kHz

Calibration

Calibrate the RFZ-5 using the SPM-16 and $R_x = R_N = 75\ \Omega$ as described in the Operating Manual. Then remove R_x and press buttons /ABS/ and /REF/ on the SPM-16 simultaneously; then press button /ABS-REF/. The 0 dB display then corresponds to $a_r = 0$ dB.

Measurement

Connect the R_x terminal of the bridge to the BB output [17] of the RMS-5. Measure the return loss for all frequencies (set on the SPM-16!) installed in the unit under test (see buttons [4]). (Important: Use a different f_M button for measurements at 83 and 93 kHz). Repeat the measurement for each of the two test voltage settings.

Specified limit value (e):	$a_r \geq 30$ dB
Test setup error (m):	
for frequencies $\leq$ 5 MHz (when a_r = 30 dB)	+0.62/-0.60 dB
for frequencies > 5 MHz (when a_r = 30 dB)	+1.17/-1.05 dB

Measurements at input "U_M external" [16]

Connect the R_x terminal of the bridge to input $U_{M\ EXT}$ [16] and press button $U_{M\ EXT}$ [12]. Measure the return loss between 25 kHz and 5.6 MHz, noting the worst value. The error conditions described above are also applicable here.

Measurements at input "U_A external" [35]

Press button $U_{A\ EXT}$ (11). Measure the output impedance by connecting the digital multimeter to the rear jack. Note any deviation from 75 Ω.

Error limits (e) (when a_r = 30 dB):	$\pm$ 4.74 Ω
Test setup error (m):	$\pm$ 0.79 Ω

Measurement at the BB output [17] with $\hat{U}_A$

RMS-5:			
Deflection voltage	$\hat{U}_A$	[10] [2]	: 3 V
Deflection frequency	f_A	[14]	: Set the highest possible deflection frequency f_A
Test voltage	U_M	[13] [2]	: 0
8050A (DVM):			
AC voltage measurement			: ON
Measuring range			: 20 V

Measure the idle voltage at the BB output [17] and note this as the reference value. Then terminate the output with an impedance of precisely 75 Ω (e.g. R_N from the RFZ-5) and measure the voltage again. Note the deviation from the nominal value $V_{idle/2}$.

Error limits (e) (when a_r = 30 dB) : ± 0.136 V
Test setup error (m) : ± 0.038 V

8.6.2 RETURN LOSS OF THE IF CONNECTIONS

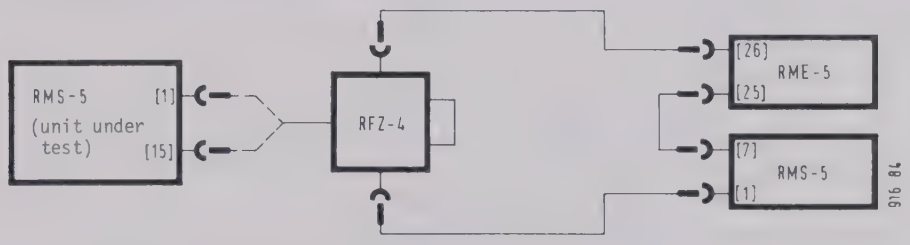


Fig. 8-2 Test setup for section 8.6.2

RM-5:			
IF measurement			
RME-5:			
IF mode		[22]	: ON
IF centre frequency		[21]	: Within the sweep range
ΔP_{II} mode		[2]	: ON
ΔP_{II} measuring range		[2]	: 10 dB/div.
RMS-5:			
IF level	P_I	[8] [2]	: -28 dBm
IF centre frequency		[9] [2]	: see table 8-15
Sweep width	$\Delta\hat{F}$	[10] [2]	: see table 8-15
Test tone deviation	Δf	[13] [2]	: 0
RMS-5 (unit under test):			
IF level	P_I	[8] [2]	: see table 8-15
IF centre frequency		[9] [2]	: Outside the respective sweep ranges as per table 8-15
Sweep width	$\Delta\hat{F}$	[10] [2]	: 0
Test tone deviation	Δf	[13] [2]	: 0

Calibration

Operate the RFZ-4 without the unit under test. Using the vertical shift [1] on the RME-5, adjust the reference line until it coincides with the centre line.

Measurement

Directly connect the Z_x terminal of the RFZ-4 to the output to be tested on the unit under test. Increase the transmission level on the RMS-5 (measuring setup) by 30 dB (+2 dBm) and read off the a_r value on the display. Note the worst values, the centre line corresponding to a_r = 30 dB.

RM-5 / Unit under test: Frequency range [10] [3]	Specified error limits (e): a_r		
	IF output [1]		IF_0 output [15] (option)
	P_{IF} = +10 dB	P_{IF} = -1 dBm	
35 MHz ± 10 MHz (option)	≥ 30 dB	≥ 34 dB	≥ 30 dB
70 MHz ± 30 MHz	≥ 30 dB	≥ 34 dB	≥ 30 dB
150 MHz ± 50 MHz (option)	≥ 26 dB	≥ 30 dB	≥ 30 dB

Table 8-15 IF return loss

Test setup error (m):
for a_r = 34 dB : +1.7/-1.5 dB
for a_r = 30 dB : +1.3/-1.2 dB
for a_r = 26 dB : ± 1.1 dB

Note: calibration must be repeated for each frequency range.

8.7 MODULATOR CHARACTERISTIC

Test equipment required:

1 receive section of RM-5	RME-5	BN 917	W&G
1 calibrated attenuator (Z = 75 Ω)	D-2053		Siemens
1 milliwatt power meter	EPM-1	BN 564	W&G
with probe	TK-10	BN 572	W&G

Modulation linearity "$U_{M\ external}$" [15]

RM-5:
IF measurement
RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: 70 MHz
Sweep width	$\Delta\hat{F}$	[10]	: 0
External test signal	$U_{M\ EXT}$	[12]	: ON

RME-5:

IF mode	[22]	: ON
IF centre frequency	[21]	: 70 MHz
Mode "Bessel zeroes"	[3]	: ON

EPM-1:

Measuring range		: ± 0.2 dBm
Output impedance	Z_{out}	: 75 Ω

Calibration level : 0 dBm

D-2053:
Attenuation : 20 dB

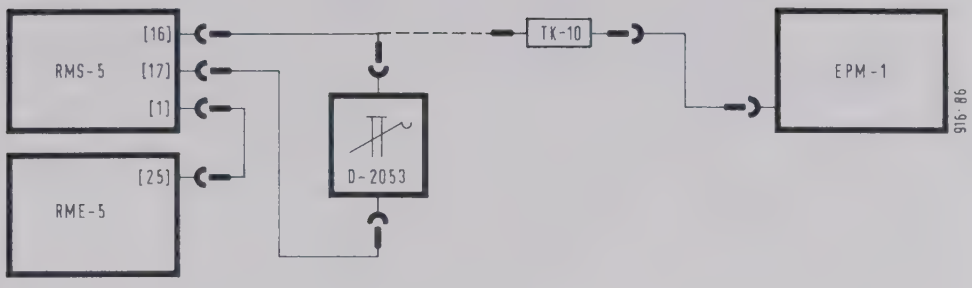


Fig. 8-3 Test setup for section 8.7, $U_{M\ ext}$

Switch on the test voltage $U_{M/mV}$ [13] on the RMS-5 and adjust it until the carrier disappears on the RME-5 (Δf_o = Bessel zero). Then connect the output of the calibrated attenuator with the probe (TK-10) of the EPM-1 and reduce the attenuation until the display is $\leq \pm$ 0.1 dBm. Calculate the attenuation of the calibrated attenuator, add the value displayed on the EPM-1 and compare the result with the nominal attenuation a_{nom} in the table ($a_{actual} = \Delta a_{cal} + \Delta L_{EPM-1}$).

Test frequency f_M [4]	250 kHz	277 kHz
Nominal attenuation a_{nom}	16.18 dB	15.26 dB
Error limits (e) ($\cong \pm$ 5%)	+0.42/-0.45 dB	+0.42/-0.45 dB
Test setup error (m)	$\pm$ 0.06 dB	$\pm$ 0.06 dB

Table 8-16 Modulation linearity "$U_{M\ external}$"

(Note: When -16.18 dBm $\cong$ 42.51 mV, the modulation linearity would be 0.4251 MHz/0.04251 V = 10 MHz/V on account of the Bessel zero at Δf_o = 425.1 kHz.)

Modulation linearity "$\hat{U}_{A\ external}$" [35]

RM-5:
IF mode

RMS-5:

IF level	P_I	[8] [2]	: 0 dBm
IF centre frequency		[9] [2]	: see table 8-17
Sweep width	$\Delta\hat{F}$	[10] [2]	: see table 8-17
Test voltage	U_M	[13] [2]	: 0

RME-5:

IF mode		[22]	: ON
IF centre frequency		[21]	: see RMS-5
ΔP_I mode		[2]	: ON

EPM-1:

Measuring range		: $\pm$ 0.2 dBm
Output impedance	Z_{out}	: 75 Ω
Calibration level		: 0 dBm

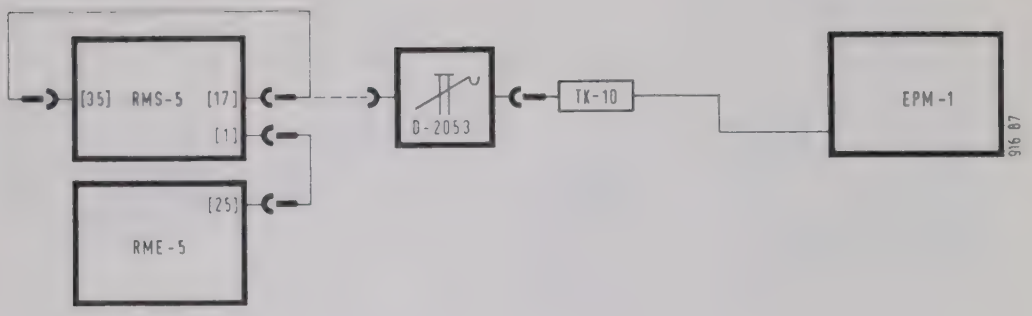


Fig. 8-4 Test setup for section 8.7, $\hat{U}_{A\ ext}$

Connect the BB output [17] of the RMS-5 with the calibrated attenuator. Set a_{nom} on the attenuator as listed in the table and adjust $\hat{U}_A$ [10] [2] until L_{nom} is displayed on the EPM-1. Then switch on $\hat{U}_{A\ EXT}$ [11] and connect the BB output with the $\hat{U}_{A\ ext}$ input [35]. Read off the ΔF value on the display and note any deviation from the nominal value ΔF_{nom}. Compare the results with the error limits specified in table 8-17. Repeat the measurement for each setting listed in the table.

IF centre frequencies [9], [2] / MHz	35 (opt.), 70, 140 (opt.)	70, 140 (opt.),	120 (for opt. 140)	170 (for opt. 140)
a_{nom} (on D-2053)	7.3 dB	17.8 dB		
L_{nom} (on EPM-1)	+ 0.025 dBm ± 0.005 dBm	-0.02 dBm ± 0.015 dBm		
ΔF_{nom}	± 9.00 MHz	± 30.0 MHz		
Error limits (e)	± 0.27 MHz	± 0.9 MHz	± 1.5 MHz	
Test setup error (m)	± 0.077 MHz	± 0.31 MHz		

Table 8-17 Modulation linearity "$\hat{U}_{A\ external}$"

0.9 V(Note: The modulation linearity would be 9 MHz/0.9 V_p = 10 MHz/V_p for ΔF = ± 9.00 MHz and $\hat{U}_A$ = (a_{nom} + L_{nom} = 7.3 dB + 0.025 dBm ≅ 0.9 V_p.)

9 FUNCTIONAL DESCRIPTION

9.1 FUNCTIONAL DESCRIPTION BASED ON THE BLOCK CIRCUIT DIAGRAM

The RMS-5 D ... comprises three main sections, namely:

BB signal generator
IF signal generator
Microprocessor control system

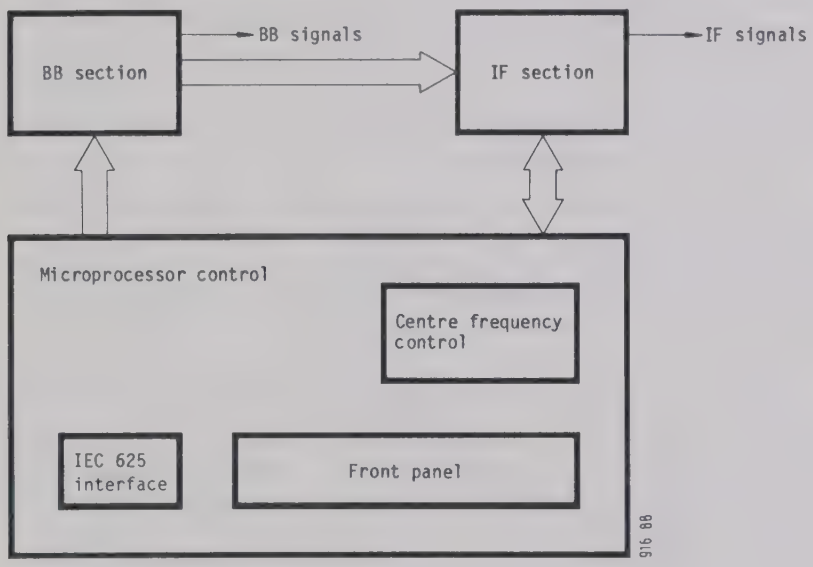


Fig. 9-1 Functional elements of the device

The BB assemblies generate the baseband signals for intermodulation measurement, the test signals (U_M) with various frequencies and the deflection signal ($\hat{U}_A$). These two signals can be drawn as a combined signal $\hat{U}_A + U_M$ and used for measurement purposes as the BB signal.

The assemblies in the IF section convert the two baseband signals $\hat{U}_A$ and U_M by means of dual modulation into the frequency-modulated and swept IF signal required. This IF signal is then available for measurement purposes.

The microprocessor control system performs three main tasks in this device. It serves the operating elements on the front panel and controls the device functions in accordance with the data entered. It also controls the device functions in accordance with the dialog conducted with an external computer via the IEC interface.

Thirdly, the microprocessor control system is used for internal control of the device. It ensures a constant centre frequency by acting as digital controller in the centre frequency control loop.

These three main sections of the RMS-5 are described below. Although the centre frequency is controlled by the microprocessor control system, this aspect is described in 9.1.2 for the IF section.

9.1.1 BB SECTION

9.1.1.1 Test signal (U_M branch)

The device has seven different test frequencies. These are subdivided into two dependent series each with five test frequencies of less than 1 MHz and two optional test frequencies of up to 5.6 MHz. The test frequencies are derived by division from a 10 MHz crystal oscillator and another oscillator with two individually switchable crystals. A 2:1 divider forms the end of the divider chain, ensuring an exact clock ratio of 0.5 (14).

The digital signal with imprecise amplitude is limited in the U_M control element, thus switching a variable current and allowing the amplitude to be adjusted. This is followed by a switchable attenuator pad of 20 dB. The test signal passes via a selective amplifier which suppresses the harmonics of the square-wave signal, a low-pass filter, an output amplifier and a 20 dB divider to the modulation oscillator (2); it then passes via a switchable 40 dB attenuator pad to the output filter (16) and the output.

9.1.1.2 Deflection voltage ($\hat{U}_A$ branch)

The required deflection voltage is generated in the $\hat{U}_A$ oscillator (9) in the form of a sinusoidal voltage with low distortion and stable amplitude. It is then split into two branches:

1. Via a D/A converter connected as a variable divider to the power amplifier, output filter (16) and output jack Bu [17].
2. As the internal sweep voltage via a switchable divider for sweep widths up to 10 MHz or, in the case of sweep widths up to 50 MHz, via a D/A converter connected as a variable divider to the frequency regulator.

The deviation is reduced automatically under program control via the two D/A converters.

9.1.2 IF SECTION

Two RF oscillators form the heart of the IF generator. The IF frequency (22.5 to 200 MHz) is obtained by mixing the carrier frequency (760 MHz) and the signal frequency (782.5 to 960 MHz).

The modulation oscillator (2) generates the carrier frequency which is modulated with the test frequency or with the noise signal for white noise measurements in wideband mode.

The sweep oscillator (10) generates the signal frequency. In contrast to the carrier frequency of the modulation oscillator, this frequency is only modulated with a low-frequency voltage and thus swept. The 1 GHz low-pass filter (11) attenuates the harmonics of the sweep oscillator to obtain a low noise signal. Matching is improved by attenuator pads in the mixer (3). Adjustment to the modulation oscillator is particularly important, since any irregularities can impair the distortion results of the modulation oscillator.

The 460 MHz low-pass filter (4) is responsible for suppression of undesired composite products, although its primary function is suppression of the residual carrier and signal.

Pre-amplifier (5) and output amplifier (6) amplify the IF level to max. +10 dBm at output P_I of the device. FED-2 attenuates the IF level by max. 60 dB in increments of 10 dB. The pre-amplifier also provides an output for the frequency divider (8) and the IF output P_{II}.

9.1.2.1 Level control circuit

The output stage (6) comprises two identical subassemblies. One branch leads to the output, the other to the test detector (12).

The IF level is compared with the reference voltage in the test detector, the control amplifier (12) passing the control voltage to the control element in the sweep oscillator (10).

The reference voltage (control voltage rectifier) is generated by a reference oscillator with stable amplitude (REF level). The amplitude of this signal is set by the controller (9) via a D/A converter connected as a variable attenuator pad so that the IF level attains the required amplitude. At the same time, the IF control element in the pre-amplifier (5) is controlled via the signal $U_{control}$ (IF control element) so that the control element in the sweep oscillator need only align the attenuation to a small extent, with the result that:

the IF level upstream of the pre-amplifier remains largely constant, as does the noise at the device output.

This is important in wideband mode in order to prevent the base noise (measured in pW0p) from exceeding the required value over the entire IF level range.

Consequently, the control element in the sweep oscillator need only align the total frequency response and the non-linearity of the control element (5) in the pre-amplifier. Only the difference in the frequency responses of the two parallel output amplifiers and the frequency response of the rectifier form the output frequency response.

9.1.2.2 Frequency control circuit and centre frequency control

The function of the frequency control circuit is

- to maintain the centre frequency at a constant value
- to adjust the sweep oscillator so that the generated frequency deviation is proportional to the sweep voltage applied and
- to enable displacement of the IF.

The signal for the frequency divider (8) is drawn from the pre-amplifier (5). The division is 100 in the 35 MHz band, 200 in the 70 MHz band and 400 in the 140 MHz band, depending on the IF band selected by the controller.

This results in a discriminator switching frequency of 350 kHz at the centre frequency of the respective bandwidth.

The switching discriminator converts the input frequency into a proportional output voltage which is compared with the sweep voltage in the frequency regulator. The control amplifier adjusts the frequency of the sweep oscillator so that the IF output frequency corresponds to the applied sweep voltage. Centre frequency control is based on integral frequency measurement of the IFD signal over exactly one sweep period. If the discriminator is linear, each measurement corresponds to the centre frequency. An additional measurement is performed using the 350 kHz reference frequency corresponding to the centre frequency of the band, since the duration of the sweep period is not sufficiently accurate.

The IF centre frequency is obtained from the quotient of the two frequency measurements multiplied by the centre frequency of the band. A number of measurements are also averaged digitally to reduce result fluctuation and improve the resolution.

A "centre frequency" parameter is passed under program control via a D/A converter to the frequency regulator which activates the sweep oscillator.

For external U_A, the sweep period is derived at the discriminator output using a 200 Hz low-pass filter and limiting amplifier.

9.1.2.3 Wideband mode

In wideband mode, the BB input [16] is connected to the modulation oscillator with signal $BB/U_{M\ EXT}$ The frequency control circuit now has a very low limit frequency (approx. 0.1 Hz) so that a square-wave signal of 50 Hz with a droop of less than 1% can still be sent (this type of signal occurs in TV transmission). The frequency control circuit only ensures that the centre frequency remains constant.

9.1.2.4 Mode $\hat{U}_{A\ EXT}$, $U_{M\ EXT}$

Additional test requirements can be satisfied using either external deflection voltages (sweep voltages) via jack Bu [35] or external test signals via jack Bu [16].

Larger modulator sensitivity can be achieved using input voltages greater than 50 mV at jack Bu [16] than using the internal signal (e.g. 100 mV ≙ 1 MHz).

9.1.3 MICROPROCESSOR CONTROL SYSTEM

The microprocessor control system comprises the CPU board (CPU-2) with an 8085 microprocessor, ROM and RAM memories, the IEC bus interface board, the front panel with operating elements and the control board.

The dialog with the user is conducted via the operating elements on the front panel or via the IEC interface.

The control signals for the input and output gates of the operating elements are decoded on the front panel board. Interrupt RST 6.5 informs the CPU of any operator requests via the front panel.

The standard "<IEC 625> bus" assembly serves as the IEC interface. The appropriate gate control signals are again decoded on the actual assembly. Interrupt RST 7.5 informs the CPU of any operator requests via the IEC interface.

The CPU board communicates with the analog section of the RMS-5 via the control board. The control board accommodates all input and output gates, as well as the digital control elements (D/A converters) via which the device functions are controlled. The requisite control signals for this assembly are also decoded here.

RST 5.5 is generated from the signal $\hat{U}_A$ and used as the trigger for centre frequency control and passed to the CPU.

9.1.4 OPTIONS

9.1.4.1 IF calibrating generator (quiet tone)

The IF calibrating generator comprises three switchable crystal oscillators tested for very low sideband noise.

9.1.4.2 <IEC 625> bus interface

The IEC interface BN 958 adapts microprocessor-controlled devices to the internationally standardized <IEC 625> interface bus.
The brochure "INTERFACE BUS <IEC 625>" (W&G order No.: BN 6390/00.38) contains a detailed description of the bus function and of the operating principles of the interface assembly.

9.2 ELECTRICAL DESCRIPTION OF THE ASSEMBLIES

9.2.1 POWER SUPPLY UNIT NNT-3 (1) BN 844

The power supply unit comprises the following: earthed mains connector, fuse with fuse holder, voltage selector and line filter, transformer, rectifier, smoothing and regulation circuits.

The secondary voltages from the line transformer are rectified, smoothed and passed to the regulators.

The ±12 V (15 V/18 V/24 V) regulators generate the auxiliary voltages on the AC side from the regulator supply voltage via separate rectifier and smoothing circuits.

The auxiliary voltage for the 5 V regulator is drawn from the regulated +12 V (+15 V/+18 V/+24 V) output voltage in the NNT-3.

In the standard power supply unit, the rectified and smoothed voltage (unregulated voltage) may be drawn from the smoothing electrolytic capacitor at the output with the +5 V, +12 V (+15 V/+18 V/ +24 V) voltages.

The senser lines for the 5 V supply are routed to output St 2 separately from the main lines. Maximum loading of any voltage output is only possible if the other outputs are not fully loaded.

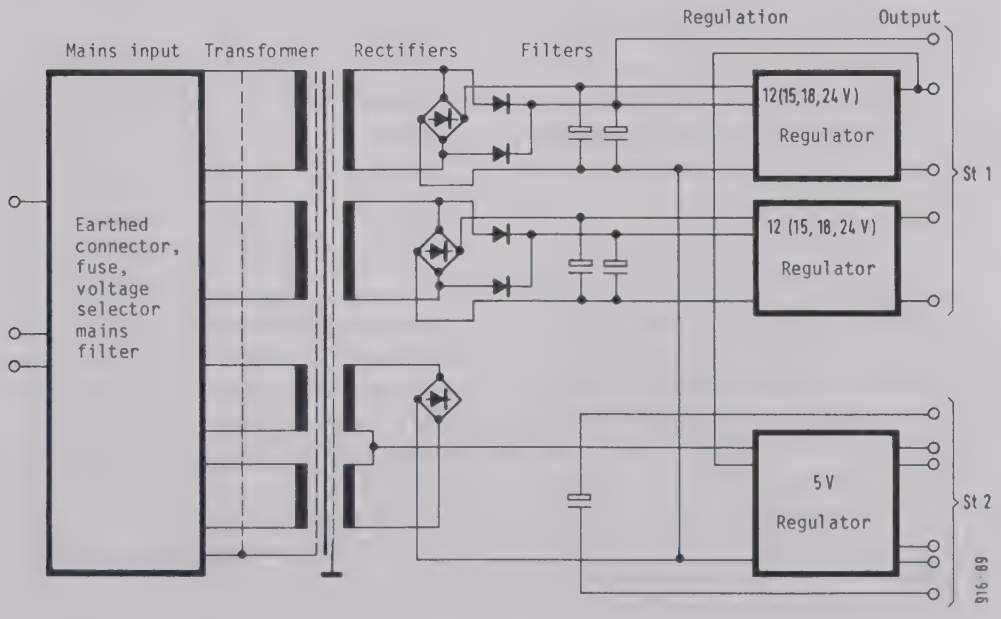


Fig. 9-2 Block circuit diagram of the power supply unit

The power supply unit of the RMS-5 includes an additional transformer winding giving a voltage of V_{rms} = 24 V which is rectified on the control board.

IC standard regulator

The following versions are available:

5 V, 12 V, 15 V, 18 V, 24 V

$I_L \leq 1.30$ A regulator L 123 + transistor stage MJE 3055

$I_L \leq 4.00$ A regulator L 123 + transistor stage BSX 45-16 + two MJE 3055 in parallel

Regulator L 123 is an integrated circuit in a TO-100 housing.

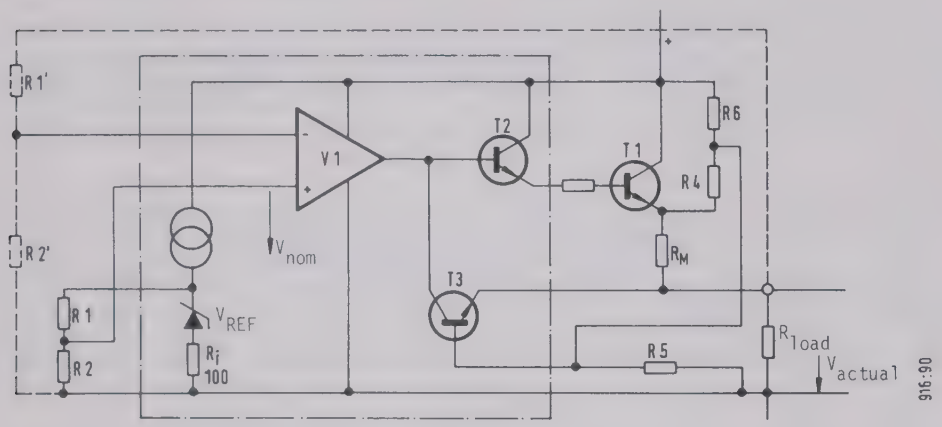


Fig. 9-3 Operation of the standard regulator IC

The standard regulator circuit comprises the following stages:

a) Differential amplifier V_1 in IC L 123-T1 compares the actual value of the output voltage with the nominal voltage at the voltage divider R 1/R 2. The voltage divider is supplied by the reference voltage V_{REF} integrated in the IC assembly.

b) The cascaded control element (T 2 in the IC, T 1 external) is controlled by the differential amplifier V_1.

c) The control element is protected by the current limitation (R 4, R 5, R 6, R_M and T 3) against thermal overloading if the output shorts.

The positive voltage V_{nom} is built up at the "+" input of the differential amplifier V_1 when the regulator is switched on. At this moment, the control element is still blocked and the output voltage equal to zero. Since the "-" input of the differential amplifier does not receive any voltage from the output and the "+" input is positive on account of "V_{nom}", the output of the differential amplifier is positively activated and the control element cleared until the output voltage at the ballast resistor V_{actual} and voltage V_{nom} match. The voltage required to drive the amplifier is negligible on account of the high gain. Resistors R 4, R 5, R 6 and R_M are dimensioned so that transistor T 3 is disabled at nominal current I_N and cannot affect the regulating properties of the circuit. The base-to-emitter voltage of transistor T 3 increases as the load current increases. This transistor conducts at 2 to 3 x I_N and absorbs the control current of the control element, causing the current in the control element to decrease and the output voltage to disappear. This is promoted by the current increase in R 6, additionally increasing the base current in T 3, thus ensuring that the output

current decreases in the event of an overload. The regulator is short circuit-proof for one minute: operation at two to three times the nominal current (just before the kink in the characteristic curve) is not permissible. The output voltage is restored automatically once the short or overload has been removed.

The magnitude of the output voltage is determined by voltage divider R 1/R 2 and the reference voltage. This is only possible if the output voltage is smaller than or equal to the reference voltage. For the 12 V, 15 V, 18 V, 24 V series, the undivided reference voltage V_{Ref} is passed to the "+" input of the differential amplifier while the voltage returned from the control element output is passed via a divider to the "-" input of the amplifier. This makes the output voltage greater than V_{Ref} by a factor of (1 + R 1'/R 2').

Battery circuit:

In the event of a power failure, the battery circuit preserves the stored data by supplying the power required. During mains operation, the three sintered batteries are charged (buffered) with a constant current derived from either the 6.5 V supply or the +12 V supply of the NNT-3, depending on the circuit design. Feedback with the mains supply on or off is prevented by two diodes (Gl 953 and Gl 952). An additional diode (Gl 954) prevents the voltage at the battery output (St 7/pt 4) from exceeding 5 V when the batteries are removed (replacement, check). The battery output is also increased to 5 V DC via T 952 during mains operation, i.e. the memories are supplied via the 5 V DC and the battery disconnected via Gl 953.
Ensure that the output is not permanently short circuit-proof during mains operation.

Data retention:

The data retention circuit generates a signal to save the stored data in the event of a power failure.

The input voltages of the 5 V and 12 V regulators are monitored using a comparator comprising IC 950 (for 12 V) and IC 951 (for 5 V). The regulator input voltages are matched to the reference voltage via the voltage dividers R 952/R 953 and R 954/R 955. The reference voltage of 2.5 V DC is obtained from the 5 V output voltage via R 950/R 951. R 956 and R 957 provide hysteresis to prevent instabilities caused by ripple on the regulator input voltage.

The output of one of the comparators switches to LOW if the input voltage drops below a minimum value (power failure).

Gl 950 is then discharged via Gl 949, T 950 is no longer on and the output for the data retention signal changes from zero to +5 V.

The time between commencement of the data retention signal and the moment when the output voltage drops below the tolerance value $V \leq 4.8$ V is 5 ms (when V_A = 5 V DC/1 A load). The data must be stored during this period. There is a delay, determined by R 958 and C 950, between switching on the a.c. line and enabling the data retention line.

Transistor T 950 will only switch on and enable the data-retention line, when the 5 V output voltage is within the specified limits.

9.2.2 SWEEP OSCILLATOR (10) AND MODULATION OSCILLATOR (2)

The sweep oscillator (signal oscillator: f = 782.5 to 982.5 MHz) is adjusted within a frequency control circuit so that an IF between 22.5 MHz and 200 MHz is obtained after combination with the modulation oscillator (carrier oscillator: f = 760 MHz).

The resonant circuit for both oscillators is a base stage with negative feedback. The collector potential is 0 V, permitting DC-free signal decoupling.

The emitter resistor receives its -12 V supply via a capacitively decoupled coaxial λ/4 line connected in series with a ferrite inductor.

This design ensures decoupling and prevents peaks and troughs in the tuning range. The same applies for the /4 lines between the oscillator circuit and the sweep or test voltage supply.

The negative feedback voltage is tapped from the collector circuit inductance (on the soldering side) and passed to the emitter via 10 C 5 and 2 C 8, a slightly higher tap supplying the output with +10 dBm into 50 ohm.

9.2.2.1 Sweep oscillator (10)

The sweep range between 782.5 and 855 MHz can be adjusted via 10 C 4, the sweep voltage being passed to pt (10) 38. The RF output voltage is passed to pt (10) 41 via a PIN diode control element.

An attenuator pad of 4.2 dB is connected between the oscillator and the pin diode control element to improve the return loss under load.

9.2.2.2 Modulation oscillator (2)

The modulation oscillator is used for modulation with the test voltage (pt (2) 46). The demand for a small linearity error (small deviation from the linear relationship between frequency and test voltage) necessitates maximum possible compliance with the relationship

$$C_{circuit} = \frac{1}{U_M^2} \times k$$

The oscillator circuit is designed so that the above relationship is approximated via an inductance parallel to 2 Gl 1 and 2 Gl 2 for a favourable working point on the characteristic curve of the tuning diodes (U_R approx. 9 V→f_{Tr} approx. 760 MHz, adjustable via P 201). This inductance can be varied to compensate the tolerances of 2 Gl 1, 2 Gl 2 and S_{22} of 2 T 1.

Additional decoupling from the oscillator circuit is achieved via 2 L 2 and the λ/4 line capacitively decoupled for RF via 2 C 10.

9.2.3 1 GHz LOW-PASS FILTER (11)

The filter concerned is a low-pass filter of the 9th order in stripline design. Its function is to increase the harmonic ratio of the signal (from the sweep oscillator) to 40 dB or more.

9.2.4 MIXER (3)

The signal frequency of 782.5 to 982.5 MHz is converted to 22.5 to 200 MHz in the ring modulator 3 IC 1. The modulation oscillator supplies the carrier input with 760 MHz (over 10 dBm_{50}).

An attenuator pad of 5.4 dB is connected between each signal or carrier input and the ring modulator in order to decrease linear distortion from mismatches. A high return loss at the carrier input of the mixer is of great importance since it considerably influences the linearity of the modulation oscillator.

Linearity is optimized by adjusting 3 C 5.

3 R 7 and 3 C 6 are used to improve mixer output matching. The mixer must be suitably matched for frequencies in the stop band of the 460 MHz low-pass filter. Distortion can be reduced by adjusting the termination (via trimmer 3 C 6).

9.2.5 460 MHz LOW-PASS FILTER (4)

The filter is designed as a stripline filter of the 9th order. Its function is to attenuate the residual carriers and signals.

9.2.6 PRE-AMPLIFIER (5)

The pre-amplifier comprises three functional units:

1. Pre-amplifier
2. Branch for P_{II} signal path

} 200 MHz amplifier

3. IF control element for P_I signal path

The pre-amplifier is matched to the 460 MHz low-pass filter via R 31 and C 31, thus allowing distortion and, to a minor extent, the frequency response of the IF path to be adjusted. The pre-amplifier comprises the circuit with T 1 and T 2. T 1 is a voltage-to-current converter for the amplifier stage with T 2. Amplification of the two stages is determined via R 6/R 3. R 2, C 1 and C 11 are required to stop the negative feedback amplifier oscillating.

The two signal paths P_I and P_{II} branch off at the output of the amplifier stage with T 2. The amplifier stages with T 3 and T 4 are designed as thin-film amplifiers to ensure that the conditions at the branch are stable, so avoiding spurious frequency responses.

The output level for signal path P_{II} can be adjusted in the amplifier stage with T 32 via P 32, the frequency response being adjusted via C 48.

The P_I signal path includes an amplifier stage with T 31 and the IF control element with Gl 31. PIN diode Gl 31 is a current-controlled RF resistor which adjusts the amplification of T 31.

Gl 31 is controlled via the control voltage "IF control element". IC 31/2 and T 36 invert the control voltage and produce a voltage offset. IC 31/1 and T 35 act as the current source for Gl 31. The IF control element is controlled by means of a table of typical setting values integrated into the device program and output via a D/A converter in (9). P 31 is used to compensate for parameter scatter in PIN diode Gl 31. The characteristic should be as accurate as possible to prevent the control element in the sweep oscillator from making unnecessary adjustments and to prevent changes in the P_{II} level. When the control circuits in the sweep oscillator have to perform level regulation frequently, the level in the mixer is unstable, and so the distortion factor of the IF signal and thermal noise are increased.

9.2.7 OUTPUT AMPLIFIER (6)

The output amplifier contains a variable gain amplifier stage to set the total gain of the IF path. For this purpose, the amplifier stage with T 1 includes a variable emitter resistor comprising R 7 and the resistor of PIN diode Gl 1. The current through Gl 1, and thus the gain, is set via P 1.

The power stage comprises two balanced amplifier sections. One section (T 2, T 4) provides the output signal, the other identical section (T 3, T 5) passes the signal to the rectifier (12). The output signal is identical to the comparison signal sent to the detector, presupposing that the drift properties of both amplifier sections are also identical.

9.2.8 FRONT PANEL (7)

The front panel comprises the following:

- Address decoders
- Display driver with LED displays
- Output gates for LEDs and piezoelectric buzzer
- Debounced keyboard

9.2.8.1 Address decoders

Address decoders IC 32 to IC 38 provide the 28 write and 4 read addresses when connected to IC 36 and IC 37. All addresses are in the I/O range 20H to 3FH. The selection signal for this range for IC 38 in circuit (9) beforehand. The front panel will only operate if control board (9) is fitted.

9.2.8.2 Display driver with LED displays

The 7-segment LED displays IC 5 to IC 17 are controlled by display drivers IC 18 to IC 30. The H-active display drivers incorporate the functions input memory, BCD to 7-segment decoding and output driver.

Individual segments, signs and decimal points are each controlled by two parallel output gates IC 51, IC 52, IC 53 and IC 40.

Parameter displays IC 3 and IC 4 are controlled via output gate IC 39 and the downstream power stages IC 31.

9.2.8.3 Output gates for LEDs and piezoelectric buzzer

The LED function indicators are controlled via output gates IC 47 to IC 50. The buzzer is driven at the appropriate frequency by IC 50.

9.2.8.4 Keyboard with debounce circuit

In the idle state, all outputs of IC 46 are LOW, while the inputs of IC 44 and IC 45 are forced HIGH by R 28 (100 kohm). When a key is pressed, one input of IC 44 is forced LOW via the key pressed and IC 46. This makes the output of IC 44 HIGH and the debouncing function is activated. When IC 44.13 is HIGH, IC 41/2 starts to count (clock frequency 500 Hz). IC 41/2 is however reset whenever a key bounce causes IC 44.13 to go LOW. When the bouncing is over and the counter reaches the value 8, it inhibits itself: IC 41.6 = HIGH. IC 43 is triggered by the positive edge and its output (RST 6.5) becomes HIGH. This signal prompts the computer to poll

the keyboard to determine which key has been pressed: the computer successively sets each output on IC 46 to LOW, the others remaining HIGH, and polls the respective input conditions of IC 45. IC 43 is then reset.

Counter IC 41/1 starts counting when the key is released. When it reaches the value 4, it disables itself and resets IC 41/2, allowing the next key operation to be registered.

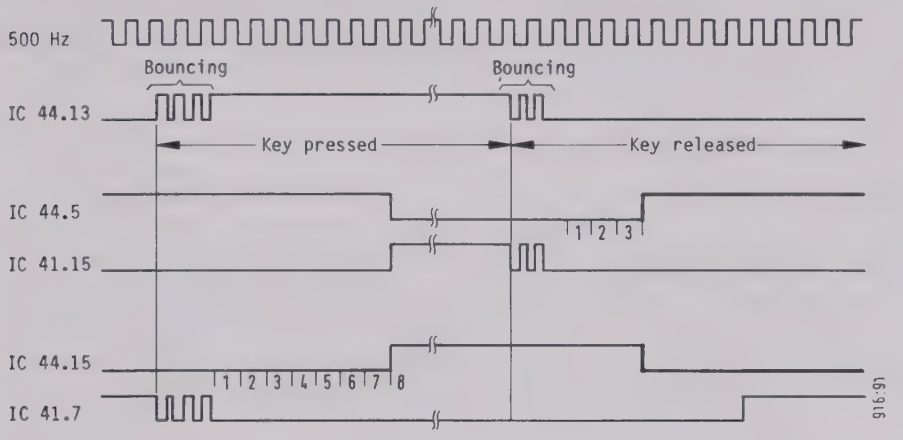


Fig. 9-4 Pulse diagram of the debouncing function

9.2.9 FREQUENCY CONTROL CIRCUIT

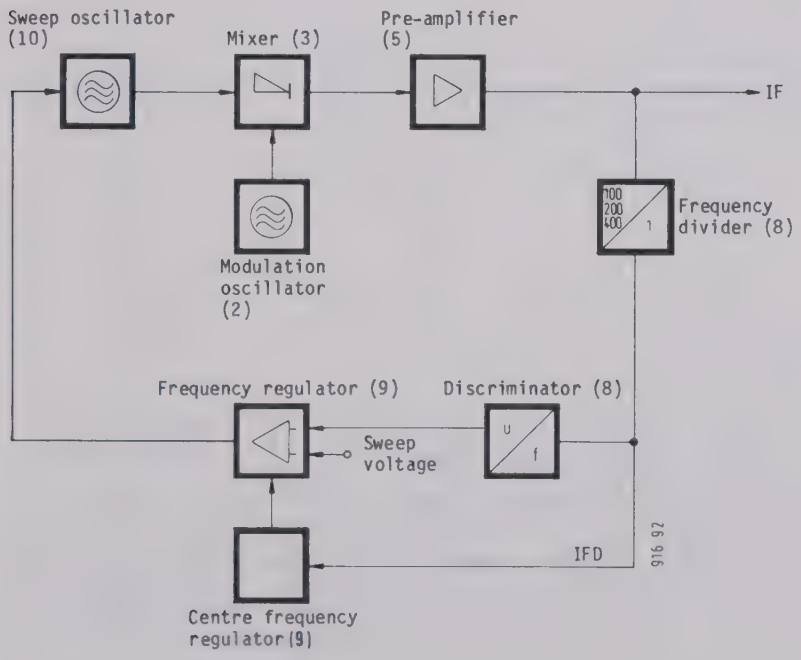


Fig. 9-5 Block circuit diagram of the frequency control circuit

The IF is obtained by mixing the two oscillator frequencies. It is amplified by the pre-amplifier and passed to the frequency divider. The latter divides the frequency in such a way as to obtain a constant discriminator input frequency of 350 kHz for IF_o = 35/70/140 MHz. The discriminator converts this frequency into a proportional voltage which is compared with a DC voltage or the sweep voltage in the control amplifier. The control amplifier adjusts the frequency of the sweep oscillator so that the difference at the input of the control amplifier becomes zero.

The frequency divider and discriminator (8), the control board (9) with frequency regulator and centre frequency control are described below.

9.2.9.1 Frequency divider (8)

The amplifier stage with T 1 matches the level to the 10 : 1 divider IC 1 and to jack Bu (7) for branching into the P_{II} path. The stage with T 2 is responsible for decoupling and matching the level for P_{II}. The divider chain provides a basic division of 100 : 1 by IC 1 and IC 2 and two divider stages of 2 : 1. The appropriately divided frequency is passed to the discriminator (or as IFD signal to the centre frequency control) by the multiplexers IC 4/1 and IC 4/2 via the selection signals IF1 and IF2, depending on the IF band selected.

9.2.9.2 Discriminator (8)

The discriminator is a switching discriminator.

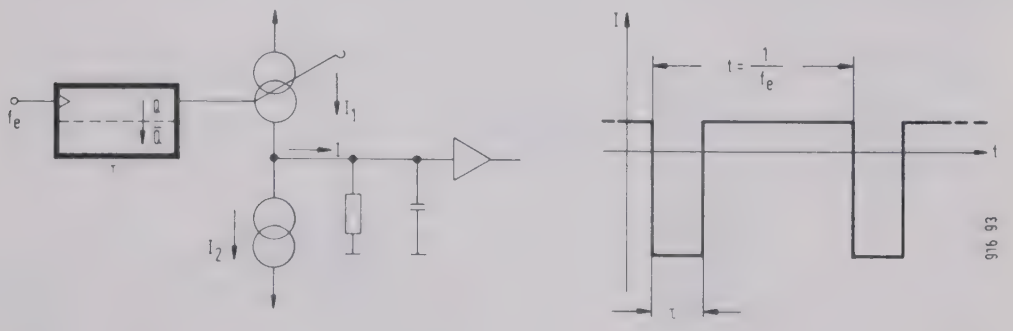


Fig. 9-6 Discriminator (8)

The conversion characteristic depends primarily on the stability of the monostable time constant and on the stability of the current sources.

The monostable time constant is determined by a "precision mono" IC 41. Current source I_1 comprises Gl 42, IC 42/1 and T 42. I_1 is switched off when T 41 is switched on in conjunction with T 43 and T 44 connected as diodes. Current source I_2 comprises Gl 43, IC 42/2 and T 45.

R 49 and C 46 form the first passive low-pass filter keeping high frequency components away from the following active filters. IC 42/3 acts as a current-to-voltage converter with frequency bandwidth limitation. IC 42.4 is a low-pass filter of the 2nd order which filters out modulation products from the test signal.

The sensitivity of the output voltage is as follows:

35 MHz band: 0.533 V/MHz
70 MHz band: 0.267 V/MHz
140 MHz band: 0.133 V/MHz

9.2.9.3 Control board (9)

The circuit comprises the following functional units:

- Address decoder
- Output gates
- D/A converters
- Level reference
- DC voltage reference
- 21 V regulator
- U_A generation
- Frequency regulator
- Centre frequency control

Address decoder, output gates, D/A converters:

IC 201 serves as pre-decoder. Address range 00H to 1FH is reserved for the IEC bus, the range 20H to 3FH being reserved for the front panel. Address range 40H to 5FH is used to select of the D/A converters IC 211 to IC 216 after further decoding by IC 204. The range from 60H to 7FH is used to select the output gates IC 205 to IC 208 after further decoding by IC 203 and the range 80H to 9FH for selection of the input gates IC 228 to IC 226 and IC 236 after further decoding by IC 202.

Output gates IC 205 to IC 208 are flipflops for driving the hardware components statically. D/A converter IC 211 is an 8-bit converter providing the control voltage for the IF control element. IC 212 is a logarithmic divider with which the level reference can be adjusted between 0.0 dB and 9.9 dB in increments of 0.1 dB. Values are entered as BCD codes in the data range from D0 to D3 and D4 to D7. IC 213 to IC 216 are 12-bit converters which can be set in four stages: loading a 3 x 4-bit word and overwriting the 12-bit word entered in the internal converter register. The converter is controlled via lines A0 and A1.

Level reference:

The level reference is a sine-wave generator with very stable amplitude and low noise. The amplitude is determined by the supply voltage V_{REF}. The frequency is exactly centred between the test frequencies of 27.7 kHz and 50 kHz in order to minimize interference to the greatest possible extent.

DC voltage reference:

The DC voltage reference IC 209 supplies +5 V. There is minor variation of voltage with temperature; the output impedance is low. IC 210 is a (+1) or (-1) amplifier, depending on the switch setting of IC 11/4, thus doubling the converter range of IC 213 (centre frequency). Slight deviations due to switching are insignificant, since the settings are incorporated into an integral regulation process.

21 V regulator:

The 21 V regulator comprises rectifier Gl 3, input capacitor C 20 and a control circuit with T 2 and T 3. The regulator is a classic circuit using the -12 V supply voltage as the reference voltage. The -21 V generated are required as the control voltage for the sweep oscillator up to 200 MHz.

$\hat{U}_A$ generation (series F onward):

The sweep frequency is either derived from the a.c. mains or from the 7 MHz crystal oscillator. Switching is via the CMOS switch 9 IC 103/2. A PLL (9 IC 104) and a switchable frequency divider circuit (9 IC 108/2, 9 IC 114 and 9 IC 113) situated in the reference loop enables the frequency of f_A to be set to the value required.

The output frequency of the PLL is 4800 times the sweep frequency and is divided down to f_A by the divider chain 9 IC 107 to 9 IC 110. To suppress the higher harmonics of the sweep frequency, the rectangular output signal of 9 IC 110 is converted to a trapezoidal signal by amplifier 9 IC 111/1, and filtered via commutating filter 9 IC 112. The switching frequency of the commutating filter is 96 x f_A, and is further attenuated by a subsequent third-order low-pass filter formed by 9 IC 111/2 and 9 R 137/9 C 29 or 9 R 200/9 C 200.

The gap pulse is generated by 9 IC 102.

The sweep voltage is adjusted with 9 P 102 with a sweep width of 9.9 MHz. To increase the resolution of the converter at small sweep widths, the 5 : 1 divider (9 R 131, 9 R 32) is switched in if the sweep width is < 10 MHz.

Frequency regulator:

The control voltage from the discriminator is inverted by IC 3/2 and its amplitude set precisely by P 1. The control voltage for the sweep width from IC 220 via IC 7/2 and IC 7/3 is matched to the varying sensitivity of the discriminator by amplifier stage IC 3/1 so that a constant sensitivity of 12 MHz/V results at the input of IC 3/1.

The input of IC 4 forms the cumulative control point. The sweep is achieved by adjusting the total current to zero via R 16 and R 17. The centre frequency is set by a DC current via R 18 and R 36. C 5 and C 6 determine the integrating characteristics of the regulator.

R 23, L 1 and C 9 suppress modulation products with the lowest test frequency of 25 and 27.7 kHz. The loop-gain changes due to the frequency divider are eliminated via divider R 29, R 30, R 31 and switch IC 9/3. Any voltage offset is made negative by amplifier stage IC 6, since the control voltage for the sweep oscillator lies between 0 V and approx. -15 V. R 44, R 45 and C 15 are used to stabilize the control circuit.

IC 8/2, R 19, IC 5/1, IC 5/2 with connection, IC 8/4, T 1 and C 16 are installed for wideband mode. Gl 1, Gl 2 and Gl 5 to Gl 7 are installed to prevent any latch-up of the CMOS switches. The maximum resonant frequency of the sweep oscillator is limited by 9 IC 6/1 and is set with 9 P 3.

Centre frequency regulator:

The centre frequency regulator comprises the two binary counters IC 245/1, IC 224 to IC 227 and IC 245/2, IC 232 to IC 235, together with their read gates IC 228 to IC 231, overflow detector IC 241/1, IC 223/1, gate time and interrupt circuit IC 11/2, IC 10, IC 11/3, IC 241/3 and IC 223/2, as well as the 350 kHz reference frequency generator OS-1 and IC 237.

The divider chain comprising IC 238 to IC 240 derives the frequency for the debouncing function (500 Hz) and the gate time of 1 : 12.5 Hz $\cong$ 80 ms for wideband regulation (from Series F).

IC 245 synchronizes the clock and chip-enable to prevent counter errors due to the delay between CE and CO following switch-off. The overflow detector is necessary since an overflow in any of the counters would result in major errors. If an overflow is detected, the measurement is rejected and the counter reset for the next measurement.

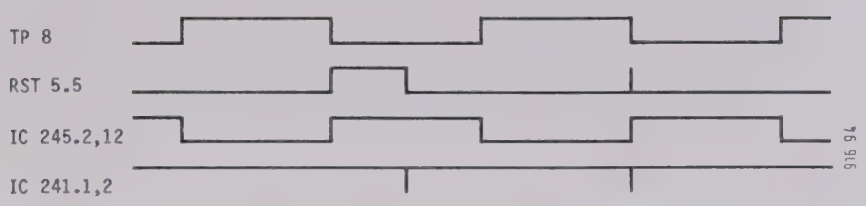


Fig. 9-7 Gate time control sequence

Every second measurement is rejected since the calculation time is approx. 25 ms, meaning that the gate times would be shorter than the period at deflection frequencies of more than 40 Hz.

In mode $U_{A\ EXT}$, the sweep period is derived from the discriminator signal via a high-pass/low -pass filter combination (C 22 to C 24, R 33 to R 35) and IC 1 via IC 11/2. IC 2 produces a logic signal when sweeping is present.

9.2.10 LEVEL REGULATION CIRCUIT

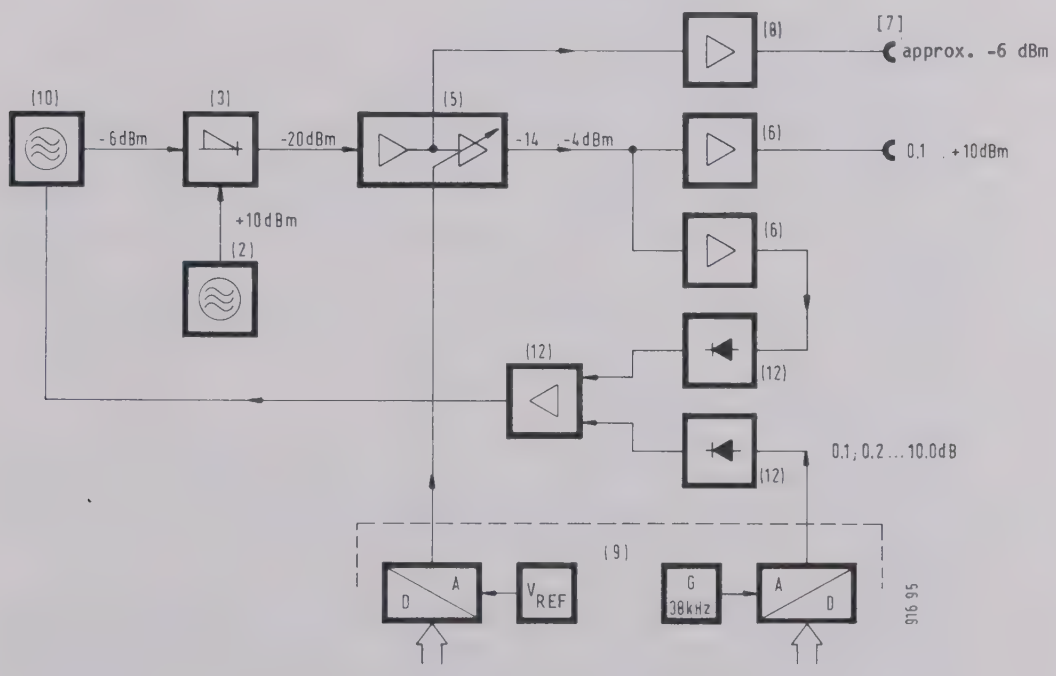


Fig. 9-8 Block circuit diagram of the level regulation circuit

The level is set using the variable gain of the pre-amplifier (5). Parameter scatter and non-linearities of the IF control element, as well as the frequency response of the IF signal path, are compensated via the detector and level regulator. This allows good level accuracies and a good frequency response to be attained in the IF output Bu [1] at the expense of auxiliary output Bu [7].

9.2.10.1 Detector (12)

The detector comprises the test branch (Gl 1, Gl 2, C 5, C 6) and the reference branch (Gl 3, Gl 4, C 4 C 7). The bias currents are determined by Gl 5, Gl 6, R 15 and R 16. All diodes have the same threshold voltage, producing a balanced current distribution.

The control voltage for the reference branch is amplified by IC 1 and T 1 and set via P 1.

IC 2 is the control amplifier whose integrating characteristics are C 9 and C 10. R 13 and C 8 suppress unwanted reference frequency components. R 18, R 19 and C 12 stabilize the control circuit. IC 3/2 is a buffer amplifier for the low-pass filter with f_g = 18 kHz and an attenuation peak at 26 kHz to suppress residual test frequencies of 25 kHz and 27.7 kHz. The gain required for stable regulation is set with IC 3/3.

9.2.11 TEST FREQUENCY GENERATION (14)

9.2.11.1 Test frequency oscillator 1

The oscillator resonates at 10 MHz. Crystal 14 Q 1 determines the frequency; 14 C 17 is connected in parallel with trimmer 14 C 20 as a load capacitor. The gain of transistor 14 T 3 is greatest at the resonant frequency, since the emitter resistor is a short-circuit for a.c. currents. The emitter and collector of 14 T 3 are 180° out of phase. Transistor 14 T 2 drives the base of 14 T 3 with the oscillator signal which is also 180° out of phase. Inductor 14 L 1 reduces the gain at lower frequencies and thus suppresses spurious resonances below the main resonance.

Transistor 14 T 5 decouples the oscillator voltage and converts it into a TTL signal.

9.2.11.2 Test frequency oscillator 2

The oscillator is transformer coupled (Meissner circuit). Crystals which provide frequency-dependent negative feed back in the emitter branch, determine the frequency. The resonant frequencies of the crystals are approx. 20 MHz and subsequently reduced to the required test frequencies in the frequency divider. The crystals are driven via resistors 14 R 22 and 14 R 25.

The various test frequencies can be accurately set via trimmer capacitors connected in series with the crystals. Crystals oscillating at harmonics are used to ensure phase stability, thus necessitating the inclusion of selection circuits in the collector branch of the oscillator. The circuit comprises the primary winding of transformer 14 O 1, capacitors being connected in parallel via control lines 14 R 10 and 14 R 16 depending on the test frequency.
Each circuit is adjusted to maximum amplitude by means of the appropriate trimmer (14 C 7, 14 C 13).

Transistor 14 T 1 and accompanying circuitry act as the operating voltage filter, particularly for low frequencies. The cutoff frequency is approx. 0.3 Hz, permitting an attenuation of approx. 44 dB at 50 Hz.

The oscillator voltage is tapped at collector 14 T 4 and passed to test point 14 TP 2 as a TTL signal via transistor stage 14 T 6.

Test frequency oscillator (2) generates the test frequencies f_{M6} and f_{M7}. Test frequencies of 2.4 and 5.6 MHz, as well as colour subcarrier frequencies of 3.58 MHz and 4.43 MHz (also unrounded values) can be provided.

The appropriate crystals and capacitors must be connected so that 14 Q 2, 14 C 18, 14 C 5 to C 7 determine the lower test frequency (f_{M6}) and 14 Q 3, 14 C 22, 14 C 11 to C 13 the higher test frequency (f_{M7}).

9.2.11.3 Test frequency divider

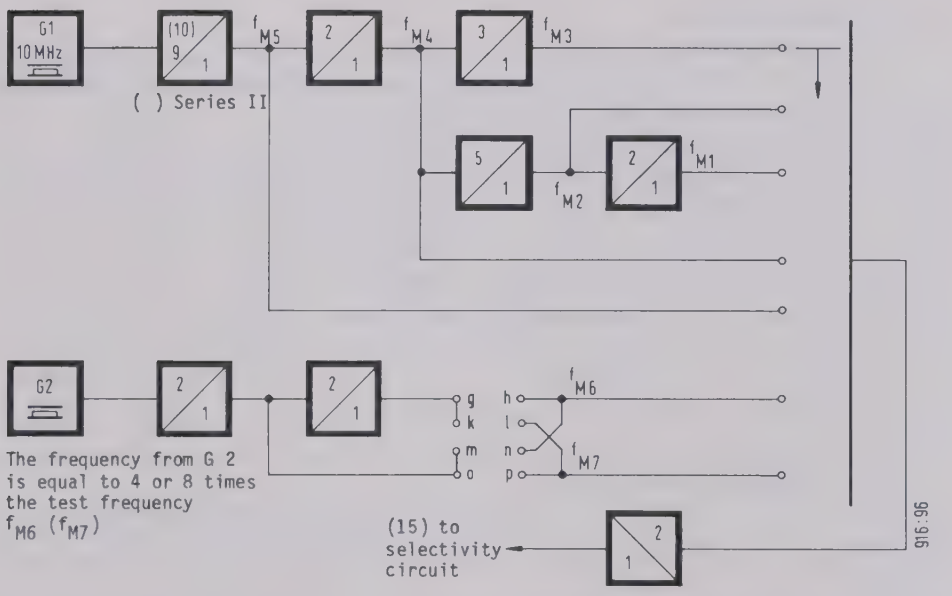


Fig. 9-9: Block circuit diagram of the test frequency divider

All test frequencies are obtained by dividing the crystal-clock frequencies of test frequency oscillators 1 and 2.

The division factor of 14 IC 1 can be altered by rewiring wire-links cd (factor 10) and ab, ef (factor 9).

Test frequency series I is derived from the division factor 9, series II from factor 10. Further division by a factor of 2, 3, 5 and 2 again results in the test frequencies f_{M1} to f_{M5} (x2) (refer to the block circuit diagram). The flipflop at the output of the assembly (14 C 4/2) balances the mark-to-space ratio.

The two higher test frequencies are derived from test frequency oscillator 2. The division factor required for the frequency concerned (in addition to factor 2 from flipflop 14 IC 4/2) can be determined by selecting the appropriate wire-links gh to op.
The appropriate gate (14 IC 8 and 14 IC 9) can be enabled for the test frequency selected by activating the relevant diode 14 Gl 11 to 14 Gl 15.
The test frequency can be disabled centrally via 14 IC 7 (0 V at (14) 89 for CAL).
Oscillator 2 is disconnected when a lower test frequency (f_{M1} to f_{M5}) is selected, only 14 IC 1 being disabled via 14 Gl 9 or Gl 10 for f_{M6} or f_{M7}. If f_{M6} or f_{M7} are switched-in, oscillator 1 is disabled by FET T 7.
A divider 14 R 47/14 R 48 at the output of 14 IC 4/2 reduces the voltage deviation before the test signal reaches pt. (14) 71 or the assembly (15).
This prevents crosstalk in assembly (15), since this would make the test voltage nonlinear.

9.2.12 U_M CONTROL ELEMENT, U_M AMPLIFIER (15)

9.2.12.1 U_M control element

The U_M control element converts the TTL signal provided by the test frequency generator (14) into a signal with variable amplitude. For this purpose, T 103 generates a current proportional to the input voltage (control voltage) U_M via IC 102 and IC 103.
This current is connected to resistor R 119 or R 120 in phase with f_M via switches T 104 and T 105 thus ensuring a continuous amplitude setting over 20 dB. A further attenuation of 20 dB can be achieved via Rel 101 and R 120. The switchable 20 dB attenuation is set to slightly smaller value by R 120 in order to permit alignment with P 101.

Following the tuning of the sweep frequency, the negative peak-value of the test voltage is reduced slightly by IC 101/3, thus obtaining a $\Delta U/U_0$ gap for setting the correct phase.

9.2.12.2 U_M amplifier

The assembly has seven individual collector stages which couple the test signal to transistor 15 T 16 via a tuned series tank circuit.

Transistor 15 T 16 is in common-base configuration; the ohmic component of the series circuit determines the input impedance. The gain of the common-base circuit is greatest at the resonant frequency.

The input impedance must be aligned to a particular value (40 Ω) via potentiometers 15 P 3 to 15 P 8 on account of the parameter scatter of the assemblies making up the input impedance of the base stage.

The collector stages 15 T 2, 15 T 4, 15 T 6, 15 T 8, 15 T 10, 15 T 12 and 15 T 14 are activated individually depending on the test frequency by the transistor stages 15 T 3, 15 T 5, 15 T 7, 15 T 9, 15 T 11, 15 T 13 and 15 T 15 in the base and collector lines. Transistors 15 T 3, etc., are enabled or disabled by the TTL signal from the control board (9). These transistors are also responsible for switching the test frequency to (14).

The selective signal passes via the low-pass filter L 10, C 26 to the output stage of the U_M amplifier which has negative feedback. The entire output stage has an approx. gain = 1 and comprises the voltage amplifiers T 18 and T 19 as well as the balanced current amplifiers T 20 and T 21. R 78 and C 32 stabilize the circuit.

9.2.13 ATTENUATION SELECTOR, OUTPUT FILTER, U_M CHANGEOVER

9.2.13.1 Output filter and attenuation selector

The deflection voltage amplified by IC 1, T 1 and T 2 is combined with U_M attenuated by 40 dB via Rel 1 to form the composite signal $\hat{U}_A + U_M$ in a high-pass/low-pass filter combination L 1, L 2, C 6, C 7. T_4 is required to prevent crosstalk when an attenuation of 40 dB has been selected.

9.2.13.2 U_M changeover

An internal or external U_M source can be selected via Rel 2. The internal U_M signal is attenuated by 26 dB via R 11, R 12 and the input impedance of the U_M changeover. C 8 acts as a high-pass filter in order to attenuate the deflection voltages further. When the external U_M source is connected, the internal signal is disconnected via a contact of Rel 2 in order to prevent crosstalk. The sensitivity of 10 MHz/V is set via P 1. A level modulation frequency response is set via P 2 and the residual 760 MHz carrier attenuated by C 11.

9.2.14 IF CALIBRATING GENERATOR 35/70/140 MHz (Opt.) (18)

The IF calibrating generator comprises three identical, switchable crystal oscillators. The crystals form a series resonant circuit with the emitter circuit of the differential amplifier concerned. The resonant circuits in the collector of T 1, T 3 or T 5 are used to set the amplitude and phase for oscillation. The resonant circuits in the collector of T 2, T 4 or T 6 reduce the distortion factor. The respective output level is set via P 1, P 2 or P 3. The appropriate oscillator level is decoupled to the base T 10 via T 7, T 8 or T 9. The collector of T 10 includes the output resistor R 40 with C 31 for setting the reflection coefficient at jack Bu [15]. The relevant oscillator with output stage via T 11, T 12 or T 13 is connected via the control lines IF1 and IF2. Wire-link TP 1 - TP 2 disconnects all oscillators, thus permitting measurement and adjustment of the reflection coefficient.

9.2.15 CPU BOARD CPU-2 (90) BN 965

9.2.15.1 Reset and power off functions

When the 5 V supply voltage is switched on, the processor is reset via the CMOS gates IC 4 while R 7, C 4 are charged. The reset state is additionally enforced as long as the POWER OFF signal from the power supply unit has not dropped to LOW. Once it has dropped to LOW, i.e. the operating voltage has reached its set-point value, R 6, C 3 must still be charged. The system starts when the output of IC 4.6 ($\overline{\text{RESET IN}}$) changes to HIGH.

When the processor writes to address 4, it resets FF IC 3, Q 4, thus itself enforcing a reset. This state is maintained as long as POWER OFF remains HIGH (even if the 5 V voltage drops).

The POWER OFF signal can be connected through to the TRAP interrupt via FF IC 3, Q 4.

Figure 9-16 illustrates the time sequence for RESET IN during the power up and power down phases. Refer to section 9.2.15.5 for further details on data recovery.

In order to ensure a perfect system reset even when switching off briefly, capacitor C 3 is discharged so quickly via diode G1 1 in conjunction with an auto-reset that the full time constant R 6, C 3 is always available when switching on.

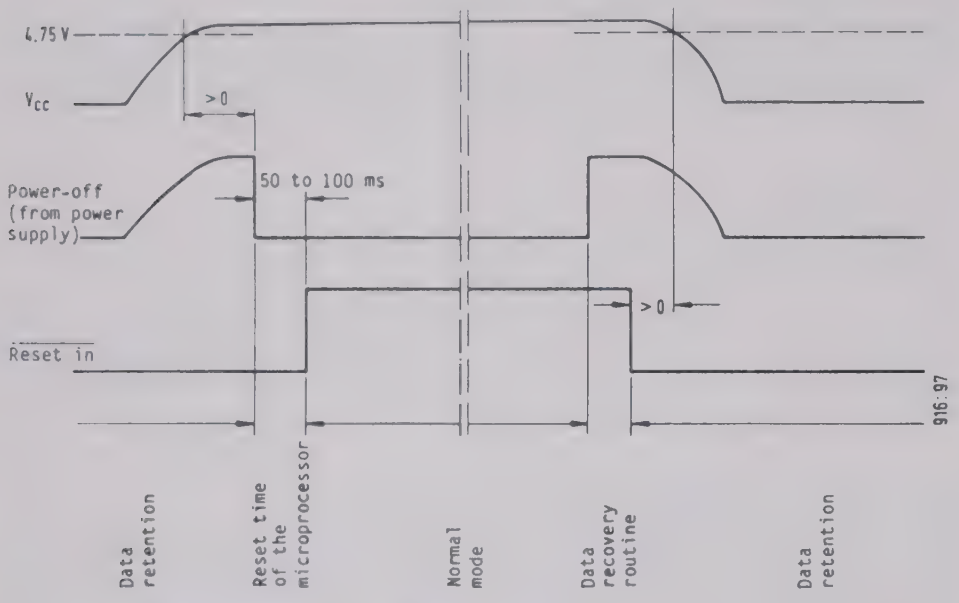


Fig. 9-10 Reset function based on POWER OFF signal

9.2.15.2 Clock generation

The 8085 processor includes an on-chip clock generator operating with an 8 MHz crystal connected between pin IC 41.1 and 2. The 4 MHz clock signal is present at pin IC 41.37.

9.2.15.3 Latches, drivers and memories

Latch IC 40 takes the addresses from the multiplex bus AD0-AD7 of the processor, making the full address and data buses available in parallel. This latch is charged by the falling edge of ALE. The address and data buses are connected to the connector strip for DMA applications or memory expansions.

In order to distribute the load due to the memories over the buses, the ROM and RAM buses are each grouped and connected to the processor via drivers IC 30 to 33 and IC 34, 37. The RAMs are also buffered separately for reasons connected with data retention (see Section 9.2.15.5).

During troubleshooting, it must be noted that RAM address drivers IC 30 and IC 31 invert. The strobe signals $\overline{RD}$ (= $\overline{OE}$) and $\overline{WR}$ are also buffered by driver IC 32.

The memories are selected via demultiplexers IC 35 and 1/2 IC 36. In the case of I/O operations or external $\overline{DISMEM}$, the memories are also deselected via these demultiplexers. The appropriate bus drivers are integrated via corresponding control lines for memory selection/no selection.

The RAM selection lines are connected via analog switches in IC 25; these are closed in normal operation (see Section 9.2.15.5).

9.2.15.4 Control lines

$\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$:

In normal mode, the processor controls the data transfer via these three control lines and the address and data buses. The lines are fitted with pullup resistors to prevent accidental read or write pulses occurring in the reset or hold states. $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ can be operated externally in the hold state.

HOLD, HOLDA:

If the HOLD input is HIGH, the processor assumes high impedance on the address and data buses, as well as on the $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ control lines. It signals this state by making output HOLDA HIGH. The program is continued when HOLD is LOW again. The LOW address latch IC 40 also assumes high impedance in parallel to the processor on account of HOLDA. The board thus has DMA capability. HOLD is a high-impedance input which must always be activated.

READY:

When this input is LOW, completion of the current read/write operations in the processor is postponed until the input becomes HIGH again, thus allowing adjustment to slower memories or peripherals. The IO bus brake and the arithmetic processor (AP) on the board use the Ready to stop the processor until their operations are completed. For this reason, Ready includes a pullup resistor R 10 and is wired AND to the bus brake and AP via the open collector gate on IC 11 (see Sections 9.2.15.9 and 9.2.15.6). External open collector circuits can also be used for braking via the connector strip.

SO, S1, ALE, RST 7.5, RST 6.5, RST 5.5, SID, SOD:

These control lines, inputs and outputs are all wired to the connector strip and only connected to the processor IC 41 (with the exception of ALE). Their function is described in the INTEL data manual. The interrupt input INTR is not available and connected to chassis-ground.

$\overline{CLEAR}$:

A negative edge causes this board input to generate a TRAP interrupt via the NAND gate IC 5.13. The $\overline{CLEAR}$ signal edge can only pass through when the POWER OFF is LOW or the inhibit flipflop IC 3, Q 3 is HIGH. The operator must ensure that inhibit FF IC 3, Q 3 is set or POWER OFF is LOW to enable the TRAP in the event of interrupt requests via $\overline{CLEAR}$.

The LOW edge of $\overline{CLEAR}$ sets the flipflop IC 3, Q 2 nevertheless; this signal can be loaded via the IO filter IC 44. This feature was included so that the program can distinguish between TRAPs triggered by the $\overline{CLEAR}$ input or POWER OFF. The $\overline{CLEAR}$ flipflop is reset by writing to address 5 via demultiplexer IC 2. The AP is reset simultaneously (see Section 9.2.15.6). A number of internal board control lines are described below:

RWIO:

RWIO becomes HIGH during read or write operations in the IO area.

$\overline{ERAM}$:

$\overline{ERAM}$ (Enable RAM) selects the highest 8K of the address area reserved for the RAM/AP.

$\overline{ER3}$:

$\overline{ER3}$ (Enable RAM 3) is the chip select for RAM 3. When the NO AP board input is HIGH, the highest 1/2K addresses are masked out from RAM 3 and made available to the AP. In this case, $\overline{ER3}$ is LOW from F800H to FDFFH.

WRRD:

This line (write or read) is the NAND connection of the $\overline{RD}$ and $\overline{WR}$ strobes. It is HIGH for every read or write operation.

9.2.15.5 Data recovery

The CMOS RAM modules permit data retention with low power consumption in idle state. Their supply voltages are therefore compiled separately to form V_{Bat} and wired for battery connection.

Fig. 9-11 Connection between U_{Bat} and 5 V supply

When switched on, rectifier Gl 6 supplies the RAMs from the 5 V supply and recharges the battery.

Changeover from normal to data retention mode:

The power supply unit sends "POWER OFF" as a warning a few milliseconds before the operating voltage drops below its minimum value. If the POWER OFF is connected through to the TRAP, an unmaskable interrupt is triggered. During the remaining time, the processor can store important data in the non-volatile RAM. Then it sets an FF, the output of which switches the $\overline{RESET\ IN}$ signal to LOW (see Section 9.2.15.1). Analog switch IC 25 then opens so that the chip select inputs of the RAMs are connected to V_{Bat} via pullup resistors R 17 to R 20.

The RAMs are protected and no leakage current can escape to the rest of the circuit via the chip select inputs. When the 5 V supply voltage eventually disappears, all RAM inputs and outputs are connected to chassis-ground by the pulldown resistors, reducing the power consumption to a minimum. The RAM area is additionally buffered to prevent the pulldown resistors from overloading the rest of the system bus.

FF IC 4.6, 4.9 generating the $\overline{RESET\ IN}$ and analog switch IC 25 are themselves connected to V_{Bat} and thus not affected by the diminishing 5 V supply. The inputs of FF IC 4.6, 4.9 are also kept in a defined state by the pulldown resistors.

Changeover from data retention to normal mode:

The power supply unit does not indicate POWER OFF LOW until the operating voltage has reached its nominal value. CMOS FF IC 4.6, 4.9 switches when the reset time R 6, C 3 expires, causing $\overline{RESET\ IN}$ to change from LOW. The processor starts up and the analog switch connects the RAM chip selects through. The time sequence is described in Section 9.2.15.1.

Checking the battery condition:

Capacitor C 2 is connected to V_{Bat} via R 3 and follows this voltage with the relatively large time constant of R 3 x C 2 approx. 8 s.

Shortly after switching on, it is possible to establish whether the battery voltage V_{Bat} was higher than the minimum limit of 3.2 V. Comparator IC 1 compares V_{Bat} at C 2 with the reference voltage derived from the 5 V supply by R 1, R 2.

The comparator output VRAM can be input to bit 0 of the IO data bus when the IO filter is switched over (UPW to LOW after writing to address 6).

This allows the processor to check whether the battery voltage was adequate to retain the data shortly before switching on.

9.2.15.6 Demultiplexer IC 2

Five $\overline{RS}$-FFs (IC 3/1 to 4 and IC 6/3/4) are installed to control these board properties; the FFs can also be switched via demultiplexer IC 2.

Demultiplexer IC 2 is activated by writing to the address area of $\overline{ROM}$ 0 and switches the FF selected via the address, since its enable inputs are connected with the ROM 0 select and the $\overline{WR}$ strobe. ROM 0 remains passive during write operations. Note that address inputs A, B and C are controlled by the inverted RAM addresses $\overline{A_0}$, $\overline{A_1}$ and $\overline{A_2}$.

9.2.15.7 Free run

When the switch settings of S 1/7 to 10 are inverted, the processor addressses the entire memory area cyclically after a reset, thus allowing the bus lines to be checked with the aid of the oscilloscope or signature analyzer. The appropriate ROM select (test point) must be used as start/stop signal in order to obtain ROM signatures. Switches S 1/7 to 10 in conjunction with the pullup resistors of the data bus and G1 2 ensure that, in the case of fetch opcode cycles, commands with the bit pattern

7	6	5	4	3	2	1	0
H	L	X	X	X	X	X	H

are read in, these representing a subset of the 8085 command set and yielding a program with consecutive memory addressing.

9.2.15.8 IO bus

The 8085 processor has input/output commands serving an internal IO data and address bus. This bus is normally used for device control. To ensure that these numerously branched lines cause as little interference as possible in sensitive circuits, W&G has incorporated a special bus concept with the following features:

- Bus transceiver
- Address bus always has a defined value and is only reversed when necessary
- Data bus maintained at the old value by the CPU board when data are not being transferred
- Special strobe signals allow address decoders and data latches/drivers to be simply connected as peripherals (see Section 9.2.15.9)
- READY' input allows IO operations to be slowed down to any rate (see Section 9.2.15.9)
- IO operations can be slowed down using binary coding via inputs B_1-B_3 within specified limits (see section 9.2.15.9).

The following capabilities are also provided:

- The IO data bus can be shorted for diagnostic purposes, i.e. the processor can reload the output data while the peripherals are disabled via the control lines.
- For special purposes (e.g. servicing), the IO read gate IC 44 and IC 45 can be switched over to read switches S 1/1 to S 1/6, the CLEAR flipflop (see section 9.2.15.4) and the VRAM signal (see section 9.2.15.5).

The IO addresses are taken from the system bus by the CMOS latch IC 39 and output continuously.

Output data are taken from the system bus by the CMOS latch IC 42 (when LSS is HIGH) and switched to the IO data bus. This is possible for both processor IN and OUT operations, meaning that, following a read operation, the data bus contains the same data as those entered. A port disable (PD) FF with the complementary outputs PD and $\overline{PD}$ can be activated via the demultiplexer IC 2. When the $\overline{PD}$ output is LOW, IO data driver IC 42 is activated continuously, allowing the data to be read from driver IC 42 during an IO read operation for diagnostic purposes. The output enable input of IC 42 is set to active LOW by $\overline{PD}$ via diode G1 4 and thus connected to control lines $\overline{RD}$ and IO/$\overline{M}$ via an OC gate IC 11.

Input data are transferred to the system bus by latch IC 43 (when IO/$\overline{M}$ is HIGH and $\overline{RD}$ is LOW). This latch is loaded with the data from filter IC 44, IC 45 by the LSS (LOW speed strobe).

Filter IC 44, IC 45 is set by flipflop IC 3 Q 1, the flipflop itself being set by demultiplexer IC 2.

9.2.15.9 IO timing control

To prevent the occurrence of IO bus conflicts due to address decoder delays in the device, the special strobe signals $\overline{RD}$', $\overline{WR}$' and $\overline{LSS}$' (LOW speed strobe) are generated on the board in addition to the IO data bus and IO address bus. $\overline{LSS}$ has AND logic and is linked to the other two strobe signals as follows:

Fig. 9-12 Generation of the $\overline{LSS}$ signal

Each IO operation is made up of three time intervals:

1. Addresses are valid: reaction time of the peripheral decoders
2. Strobe signal LOW: data transfer ($\overline{RD}$ or $\overline{WR}$)
3. Waiting time: settling time of the peripheral decoders

The three time intervals can be varied (independently) via the three board inputs B 1 to 3. B 1-3 is a 3-bit number with positive logic:

$$n = < B\,3, B\,2, B\,1 >\ ,\ 0 \leq n \leq 7$$

This yields the following timing diagram for the IO strobe signals, IO data bus and IO data adress bus:

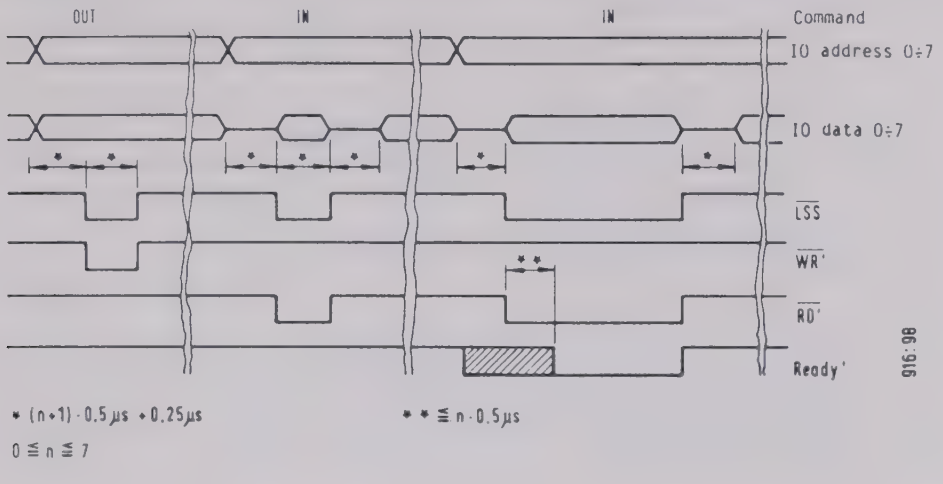


Fig. 9-13 IO timing

Interval 2 can be extended to any length through READY' LOW.

Timing control sequence

FF IC 8 and IC 9/1/2 are reset with the ALE signal. As soon as an address for the IO area is present on the data bus (IO/$\overline{M}$ = HIGH), this causes the READY signal to switch to LOW via IC 10.8 and IC 11.4. Since the $\overline{Load}$ signal (IC 7.11) is LOW, counter IC 7 already has a value of OAH (n = 5), for example. The clock pulse for counter IC 7 is enabled with READY. As soon as the counter overflows, FF IC 8/1/2 (Q = IC 8.2) is set with the next negative signal edge. IC 9 (Q = IC 9.5) is connected downstream as a shift register cell ensuring that the counter receives a $\overline{Load}$ signal with the next-but-one signal edge.

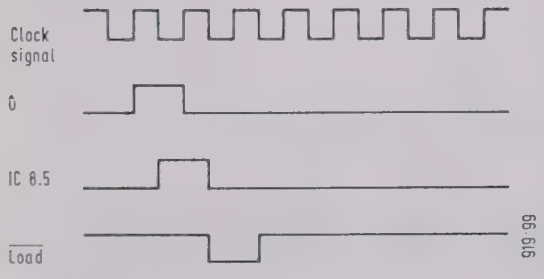


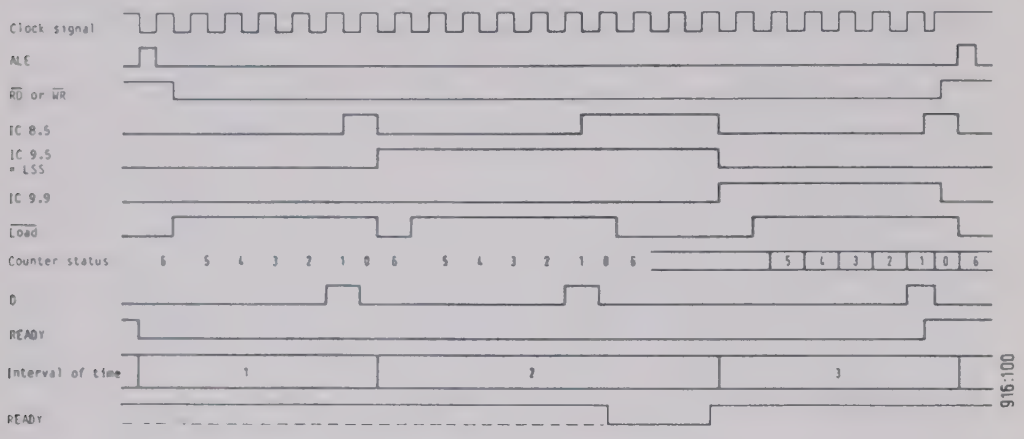
Fig. 9-14 Signal sequence for counter overflow

This sequence is repeated for every time interval.

FF IC 9 (Q = Q 2 = IC 9.5 = LSS) is set at the end of the first time interval, i.e. after the first overflow. It is reset after the second overflow and FF IC 9 (Q = Q 3 = IC 9.9) set.

With the third and last overflow, the READY signal is set to HIGH (waiting status cancelled) via IC 10.8 and IC 11.4 and the clock pulse disabled. The slowed-down procedure is also terminated.

The control signal RWIO present at IC 9.10 resets IC 9 (Q = LSS) and simultaneously fulfills a protective function: LSS pulses can only be generated when the processor wishes to read or write.



Interval 2 can be extended to any length with READY'. Counter IC 7 is loaded with data B_1-B_3 at the start of each time interval.

Fig. 9-15: Timing control sequences, general case

9.2.15.10 Test points

The board accommodates 2 x 8 test points:

Designation	Signal
$\overline{OE}$	Output Enable for ROMs, corresponds to $\overline{RD}$ strobe
ROM 0	Chip Select, ROM 0
ROM 1	Chip Select, ROM 1
ROM 2	Chip Select, ROM 2
ROM 3	Chip Select, ROM 3
ROM 4	Chip Select, ROM 4
ROM 5	Chip Select, ROM 5
ROM 6	Chip Select, ROM 6
RAM 3	Chip Select, RAM 3
RAM 2	Chip Select, RAM 2
RAM 1	Chip Select, RAM 1
RAM 0	Chip Select, RAM 0
TP 4	$\overline{LSS}$ (Low speed strobe)
TP 3	$\overline{WR}$' (Write strobe IO bus)
TP 2	SOD (Serial output data from processor)
TP 1	$\overline{RD}$' (Read strobe IO bus)

Table 9-1 Test points on the CPU board

9.2.16 <IEC 625> BUS INTERFACE (91) BN 958

The IEC bus interface adapts microprocessor-controlled devices to the internationally standardized interface bus <IEC 625>, known as the IEC bus.

9.2.16.1 Functional description based on the block circuit diagram

For the microprocessor, the IEC bus interface represents a collection of input and output gates. Data are exchanged between the IEC bus and the device via these gates.

The data transfer between IEC bus and device is controlled by the IEC bus program. The PROMs in which this program is stored are located in the device and not on the IEC bus interface board.

The actual interface logic is located in the Motorola IEC bus interface assembly MC 68488. The majority of interface functions are performed independently by this assembly, i.e. without reference to the microprocessor in the device. The IEC bus handshaking cycle, for instance, is handled independently and all messages sent to the IEC bus are decoded by the assembly.

The interface status assumed on the basis of these messages is written to the corresponding input gates.

A further input gate acts as transfer register for listener bytes. Listener bytes are the data transferred from the IEC bus to the device when the device is addressed as listener, i.e. when setup parameters for the device are being transferred.

The assembly also includes output gates in addition to the input gates.

Their functions are as follows:

- They receive control commands which the microprocessor uses to influence the interface logic (e.g. it can halt the handshaking cycle or send a service request SRQ via the IEC bus).
- They act as transfer registers for bytes to be transferred from the device to the IEC bus, such as talker bytes and status bytes. Talker bytes are the data transferred from the device to the IEC bus when the device is acting as talker, e.g. when measured values are being transferred.
  The status byte is the device's reply to a serial poll and contains the current device status.

  The "address" switch is used to set the device address.

  The "PP message" switch is used to determine the data line from the IEC bus on which the device is to send its status bit RQS (requested service) in reply to a parallel poll by the controller.

  The internal microprocessor must have access to certain IEC bus lines in order to allow the IEC bus interface BN 958 to be used as the actual IEC bus controller. These lines can be accessed via the controller input and output gate.

Interworking of instrument and IEC bus interface

When the IEC bus assumes a status requiring service by the internal microprocessor, the IEC bus interface sends an interrupt to the device. This interrupt causes the microprocessor to execute the IEC bus program. Such a situation may arise if:

- the device is to be switched from local to remote control or vice versa;

- a listener byte is sent via the IEC bus. The interface logic writes this byte to the transfer register for listener bytes and halts the handshaking cycle. Handshaking remains interrupted until the microprocessor reads this byte (IEC bus line NDAC = HIGH). Once the listener byte has been processed and stored, IEC bus line NRFD also becomes HIGH.
- the device is to provide a new talker byte. The IEC bus line DAV becomes LOW to start the handshaking cycle when the new talker byte is written to the appropriate output gate.
- the device is to perform a measurement in response to the IEC bus command "Device Trigger (GET)". This causes the interface logic to halt the handshaking cycle until the microprocessor starts the measurement and the handshaking cycle is re-enabled (NDAC = HIGH and NRFD = HIGH).
- the device is to assume a defined initial status in response to the IEC bus command "Device Clear (DCL or SDC). This also causes the interface logic to halt the handshaking cycle until the microprocessor resets the device to its intitial status and the handshaking cycle is re-enabled (NDAC = HIGH and NRFD = HIGH).

If wirestrap CLR is fitted on the IEC bus interface board, the IEC bus signal IFC (Interface Clear) causes the device to be initialized. This ensures that the device can always be initialized via the IEC bus in the event of a lock-up. (This is important for devices in unmanned stations where a lock-up resulting from external causes cannot be cancelled by switching the mains power off and on again.)

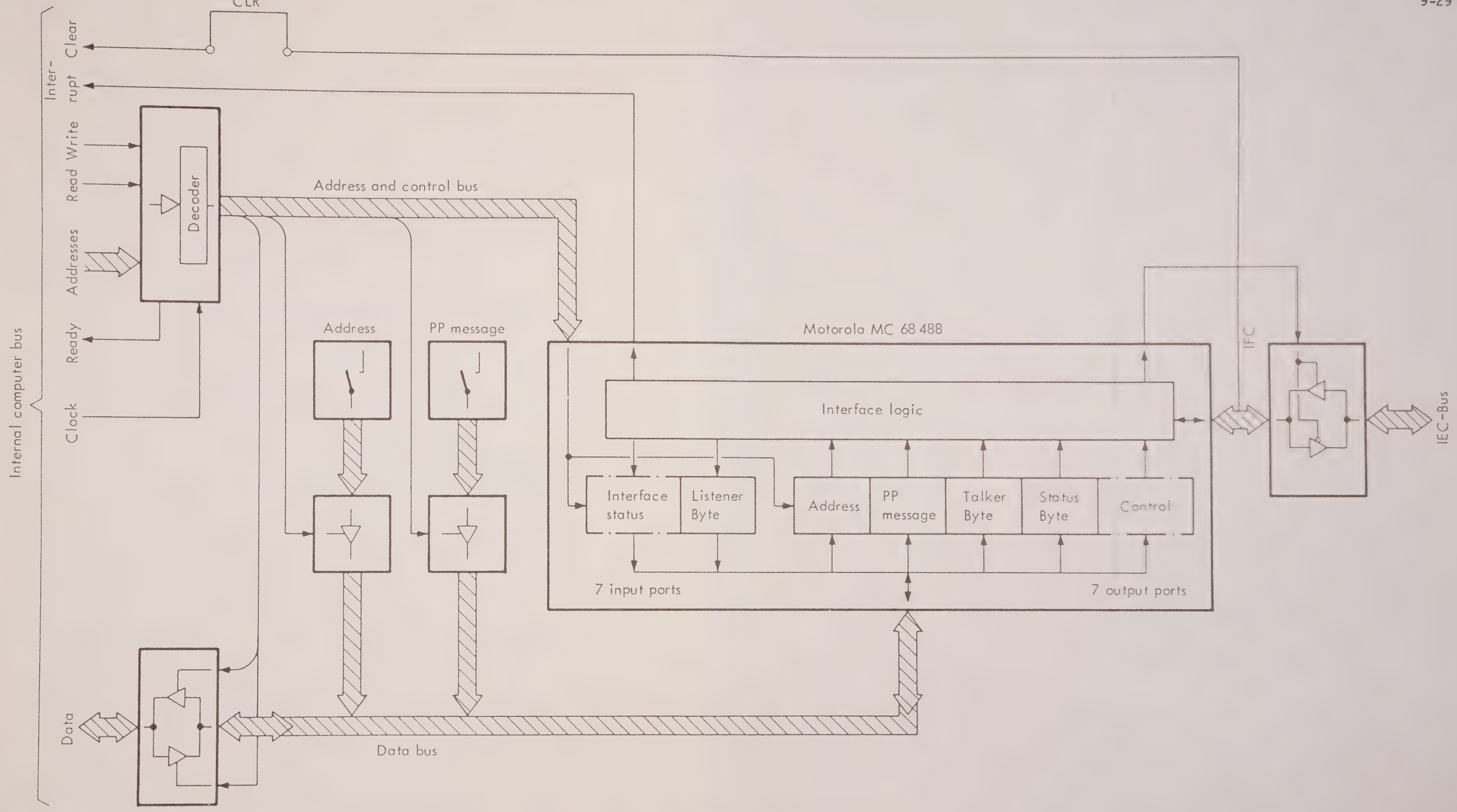


Fig. 9-16 Block circuit diagram of the <IEC 625> bus board

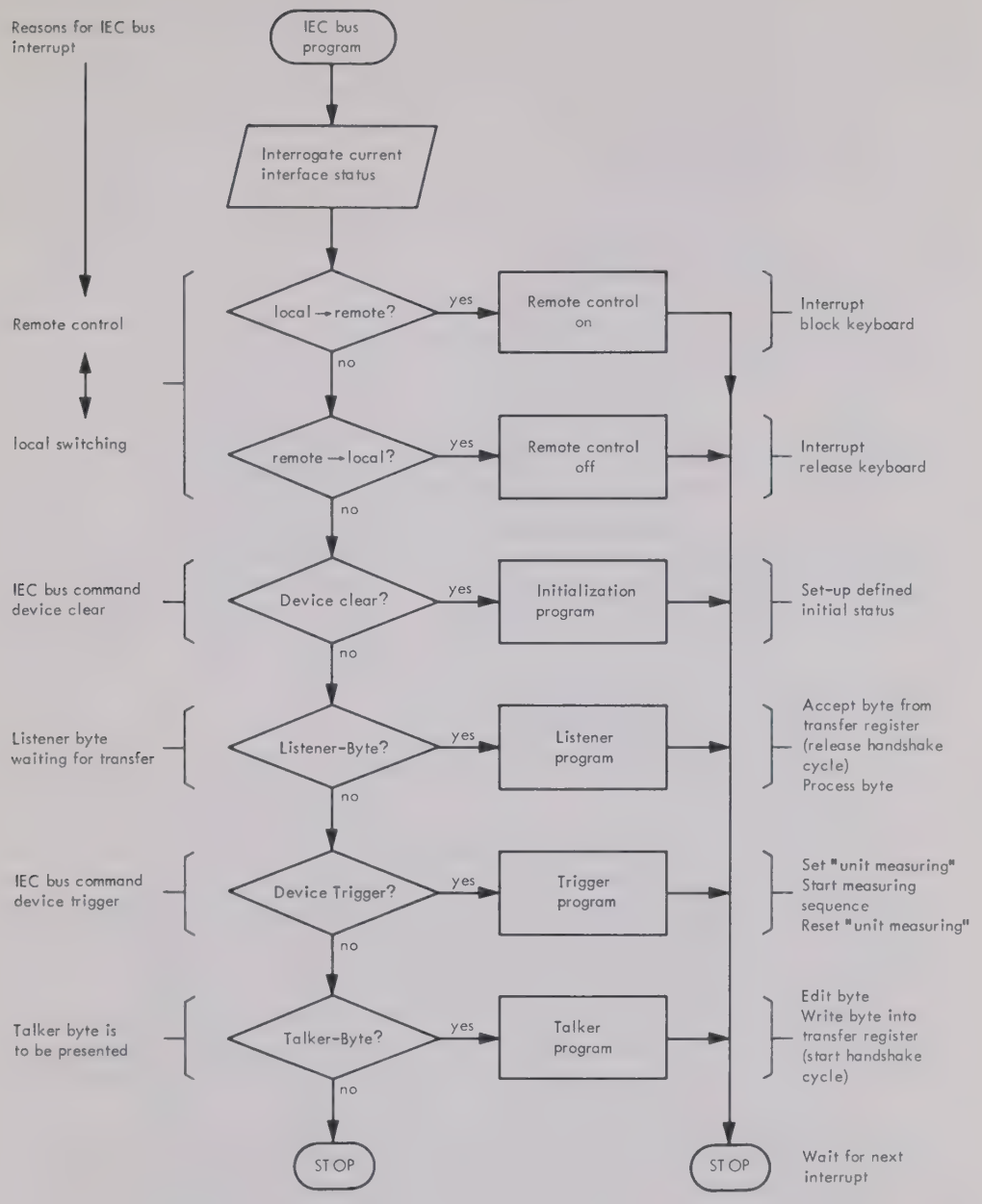


Fig. 9-17 Structure of the IEC bus program

9.3 SOFTWARE DESCRIPTION

9.3.1 LIST OF TEST ROUTINES

These are described in Section 7.

9.3.1.1 Test routines for the CPU board

- ROM test
- RAM test (without modification of memory contents)
- RAM test (with modification of memory contents)
- IEC test
- I/O test
- Summary self-test (cyclic test run including: ROM test, I/O test and RAM test without modification of memory contents)

If the summary self-test reveals an error, an error message is output to the front panel. As in all the test routines, detection of an error or fault causes the program run to be interrupted, as indicated by the SOD signal.

9.3.1.2 Test routines for device hardware

I/O ports (signature analysis, PORT 1, PORT 2)

Centre frequency control (self-test and signature analysis)

Frequency control linearity (self-test)

D/A converter, functional test for the following signals:

$\hat{U}_A$	Centre frequency
$\Delta\hat{F}$	Rectifier control voltage
Δf, U_M	Control voltage for IF control element

9.3.2 DEVICE SOFTWARE STRUCTURE

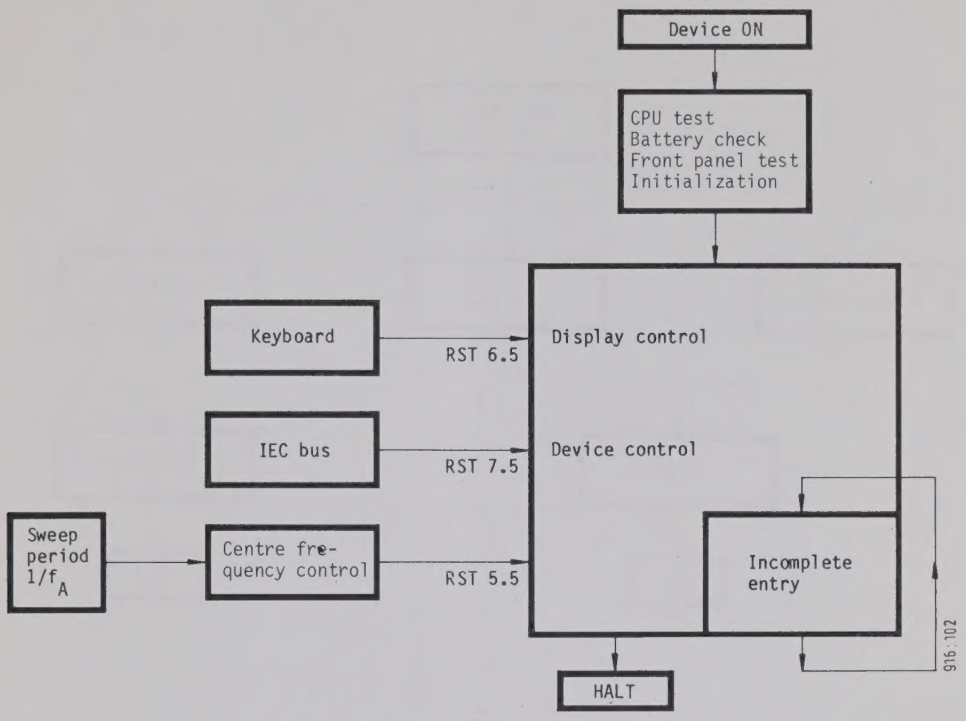


Fig. 9-18 Device software structure

The device program is normally used for establishing the front panel display and device hardware setups. The only exception to this rule is an operating status in which parameter input is not complete. This is indicated by continuous flashing of the push-button LEDs under program control.

Centre frequency regulation with a cycle time of $1/f_A$ gives rise to a regular program run which also ends in HALT status like all the other program sections.

9.3.3 BASIC PRINCIPLES OF CENTRE FREQUENCY CONTROL

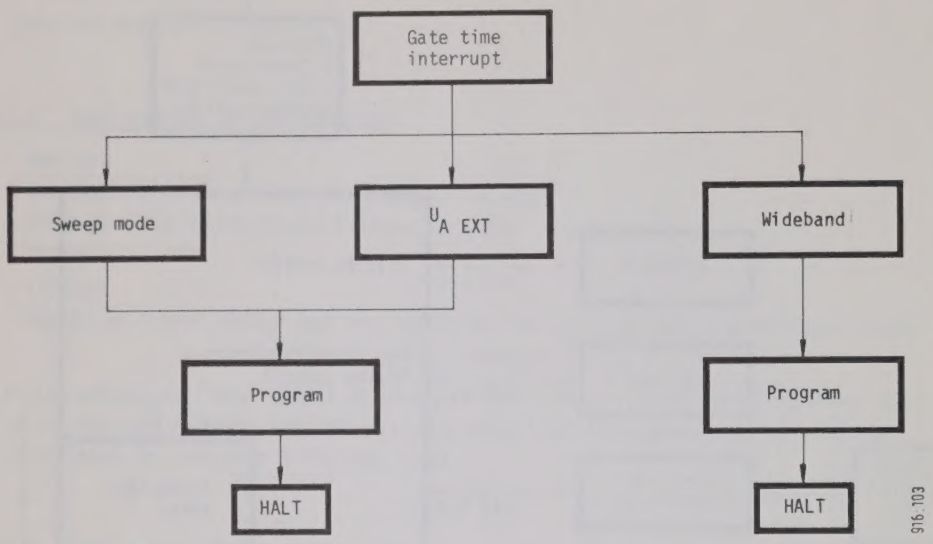


Fig. 9-19 Basic principles of centre frequency control

Sweep mode

Interrupt RST 5.5 is set at the end of every frequency measurement. The values of both counters are entered into the CPU and the instantaneous centre frequency calculated. This value is compared with the nominal centre frequency entered via the keyboard; if necessary, a correction value is determined and output for the centre frequency signal. Interrupt RST 5.5 is subsequently reset.

The correction value is averaged digitally since the frequency measurement resolution is smaller than that of the output converter. In order to prevent falsified measuring times from being evaluated, only each alternate measurement is read in and the interrupt reset immediately without a correction value being determined.

An identifying signal (UAE) is evaluated in mode $U_{A\ EXT}$. If this signal is set, there is a sweep capable of evaluation. The sweep period is derived from the external or internal f_A, depending on the state of this signal.

In all other respects, the control sequence is as for sweep mode.

Wideband mode

In wideband mode, the entire frequency control circuit is used only to stabilize the centre frequency. The frequency regulator has a very low limit frequency. The gate time for frequency measurement is set at 1/12.5 Hz = 80 ms. The frequency measurements are performed in rapid succession with only short intervals for storing the values, thus improving the sampling conditions. The frequency measurements also yield a correction value which is again averaged digitally and output.

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